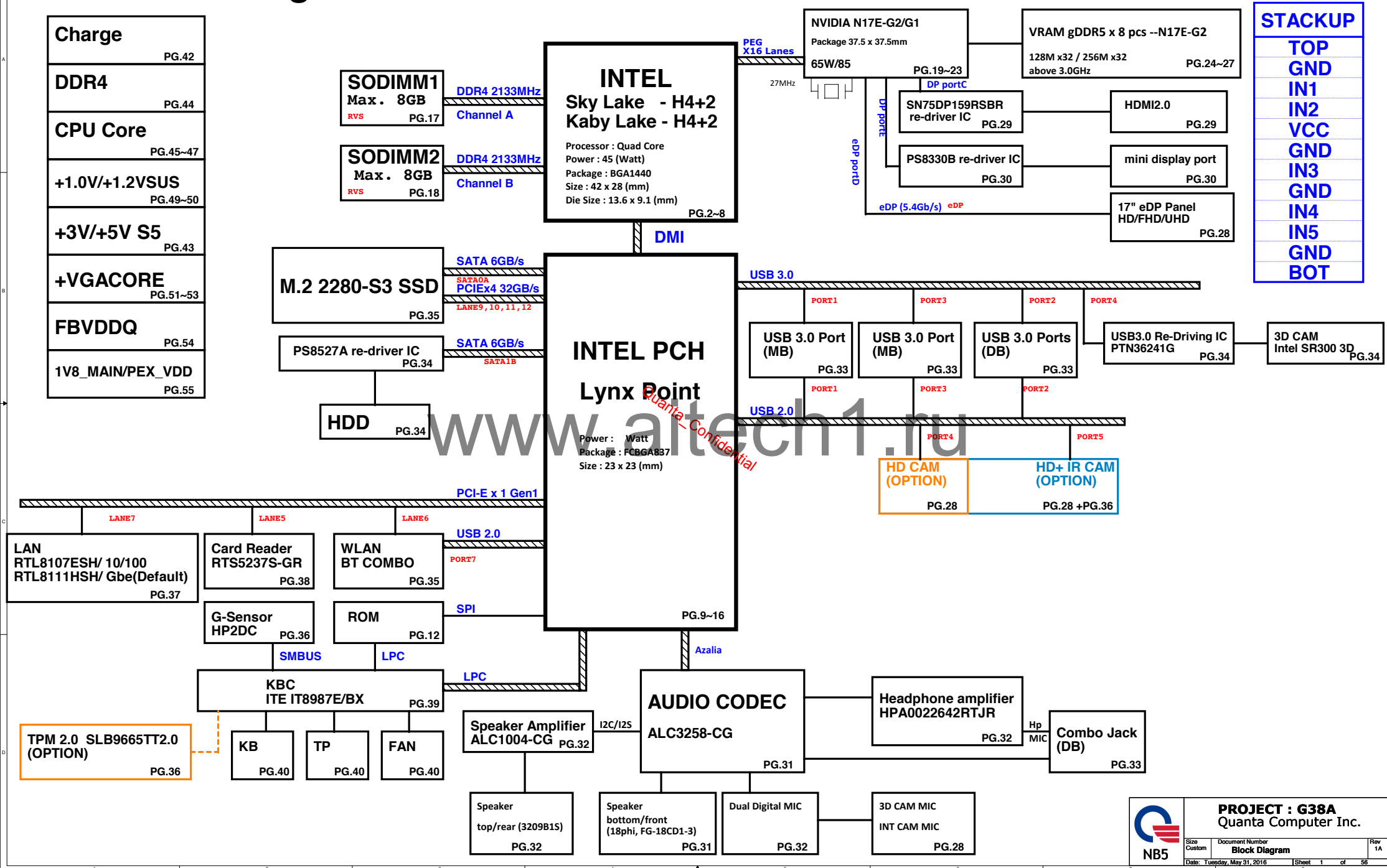


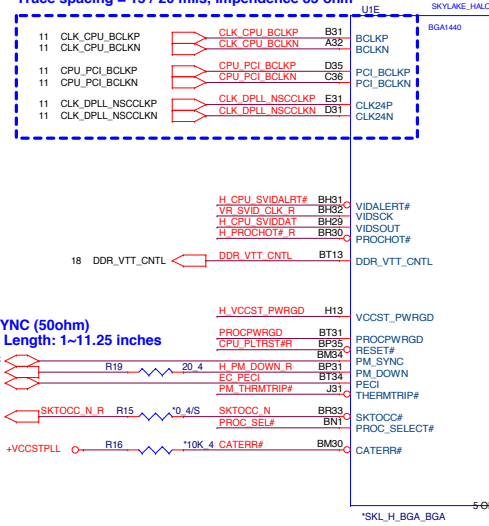
# Pavilion Gaming Griffin1.1 INTEL SKL / KABY -H SYSTEM DIAGRAM

01

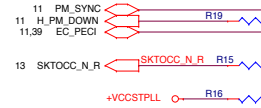


## SKYLAKE Processor (CLK, MISC, JTAG)

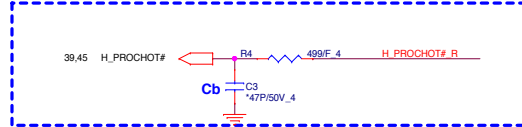
Host CLK:  
Trace length < 11000 mils  
Trace spacing = 15 / 20 mils, Impedance 85 ohm



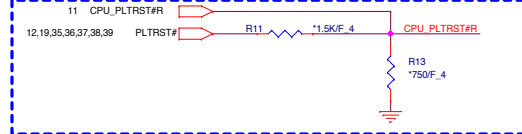
PM\_SYNC (50ohm)  
Trace Length: 1~11.25 inches



PROCHOT# (50ohm)  
Trace Length < 11 inches  
Cb need placement near VR



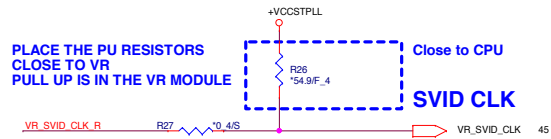
CPU\_PLTRST# (50ohm)  
Trace Length: 10~17 inches



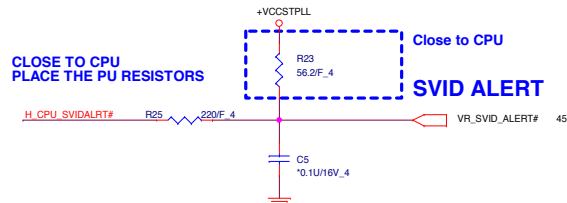
## CPU CORE SVID

Layout note:  
1. Need routing together  
2. ALERT need between CLK and DATA.

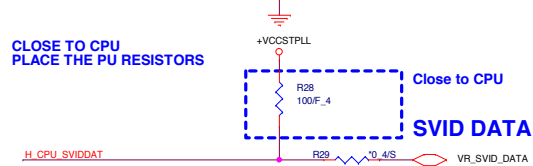
PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE



CLOSE TO CPU  
PLACE THE PU RESISTORS



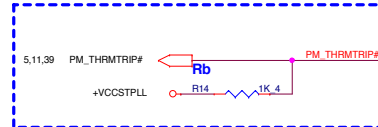
CLOSE TO CPU  
PLACE THE PU RESISTORS



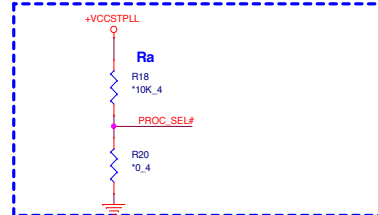
PROCPWRGD (50ohm)  
Trace Length: 1~11.25 inches



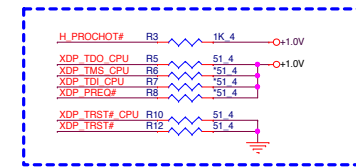
THERMTRIP# (50ohm)  
Trace Length: 1.1~12 inches  
Rb need placement near PCH



Ra(R18) Not install in SKL-H



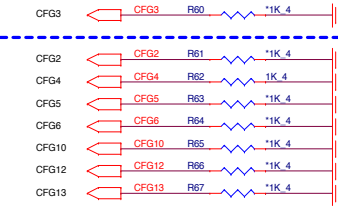
## Processor pull-up (CPU)



## Processor Strapping

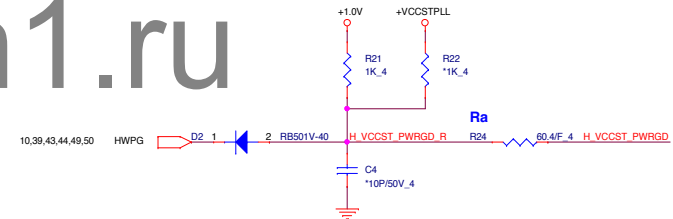
The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX\_ENABLED BIT IN DEBUG  
1, Disable;



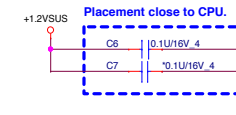
## HWPD

Ra close to CPU side  
H\_VCCST\_PWRGD trace 0.3" - 1.5"

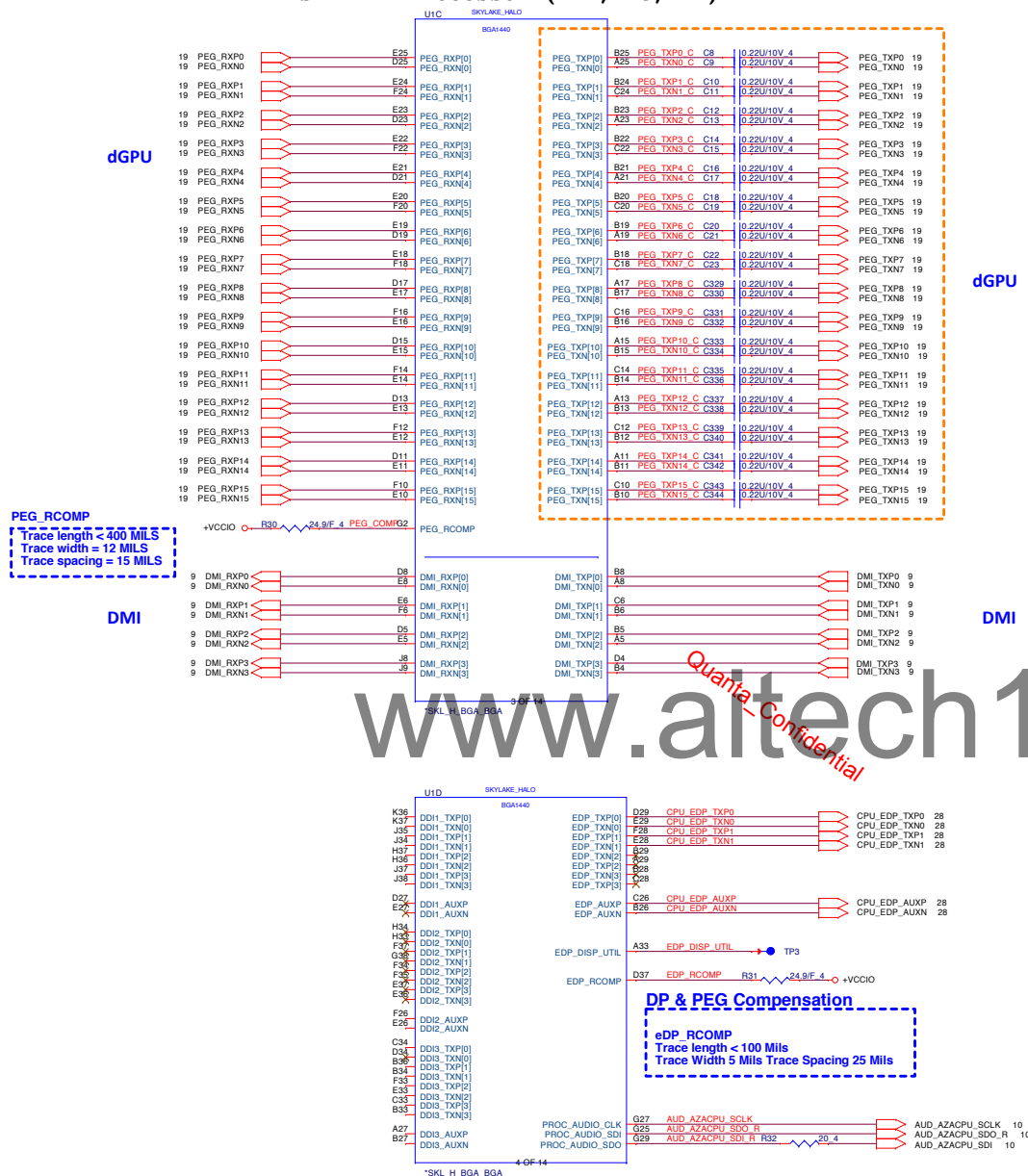


## CPU VDDQ

Note: please keep plane is enough for VDDQ 2.8A

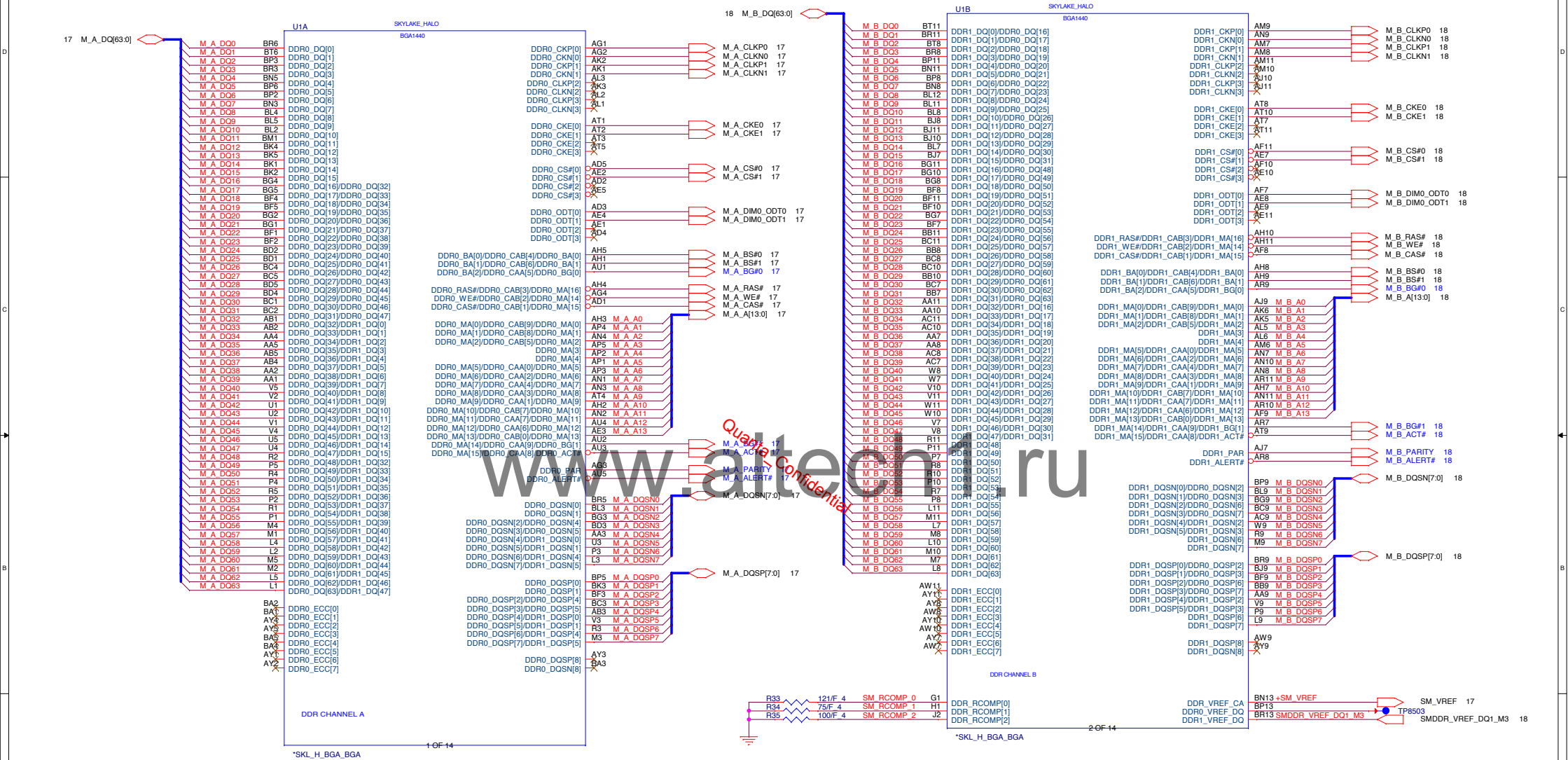


## SKYLAKE Processor (DMI, PEG, FDI)



+1.2VSUS 2.6,10,17,18,44,50,55  
 +3VS5 10,12,14,16,28,29,30,35,39,43,44  
 +3V 5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35

## SKYLAKE Processor (DDR4)





## SKYLAKE Processor (POWER)

Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A

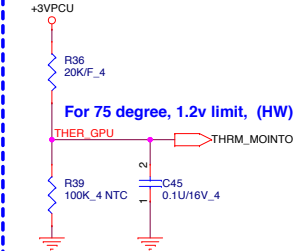
+VCC\_CORE 7,45,46  
+1.2VSUS 2,6,10,17,18,44,50,55



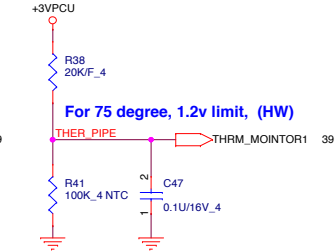
## IO Thrm Protect

Location need thermal confirm

## For GPU USE

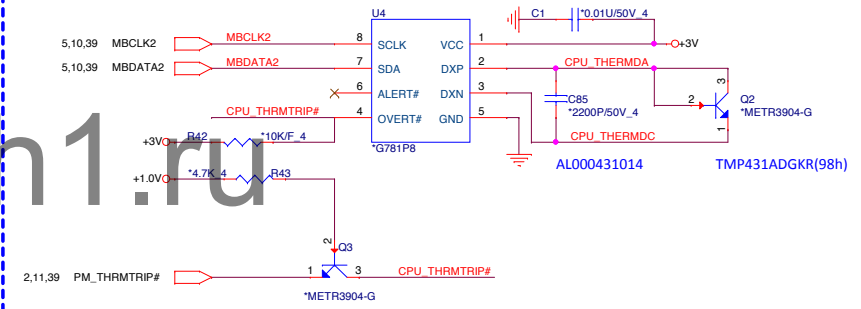


## For PIPE USE

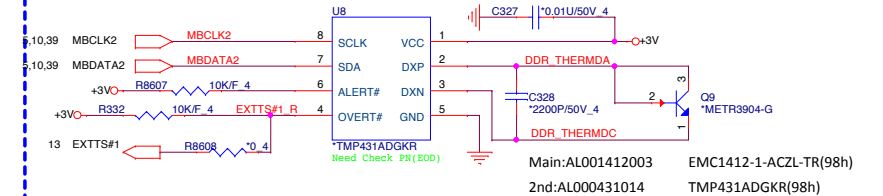


## CPU Thermal Sensor

Location need thermal confirm



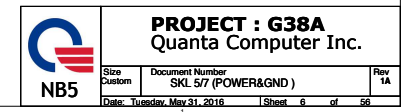
## GPU Thermal Sensor



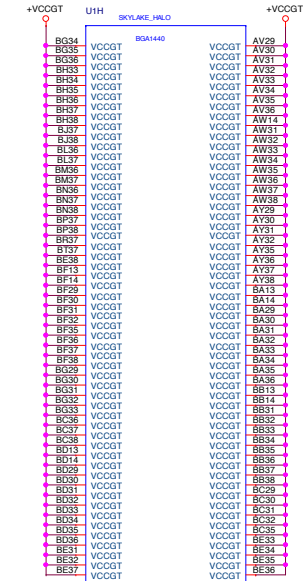
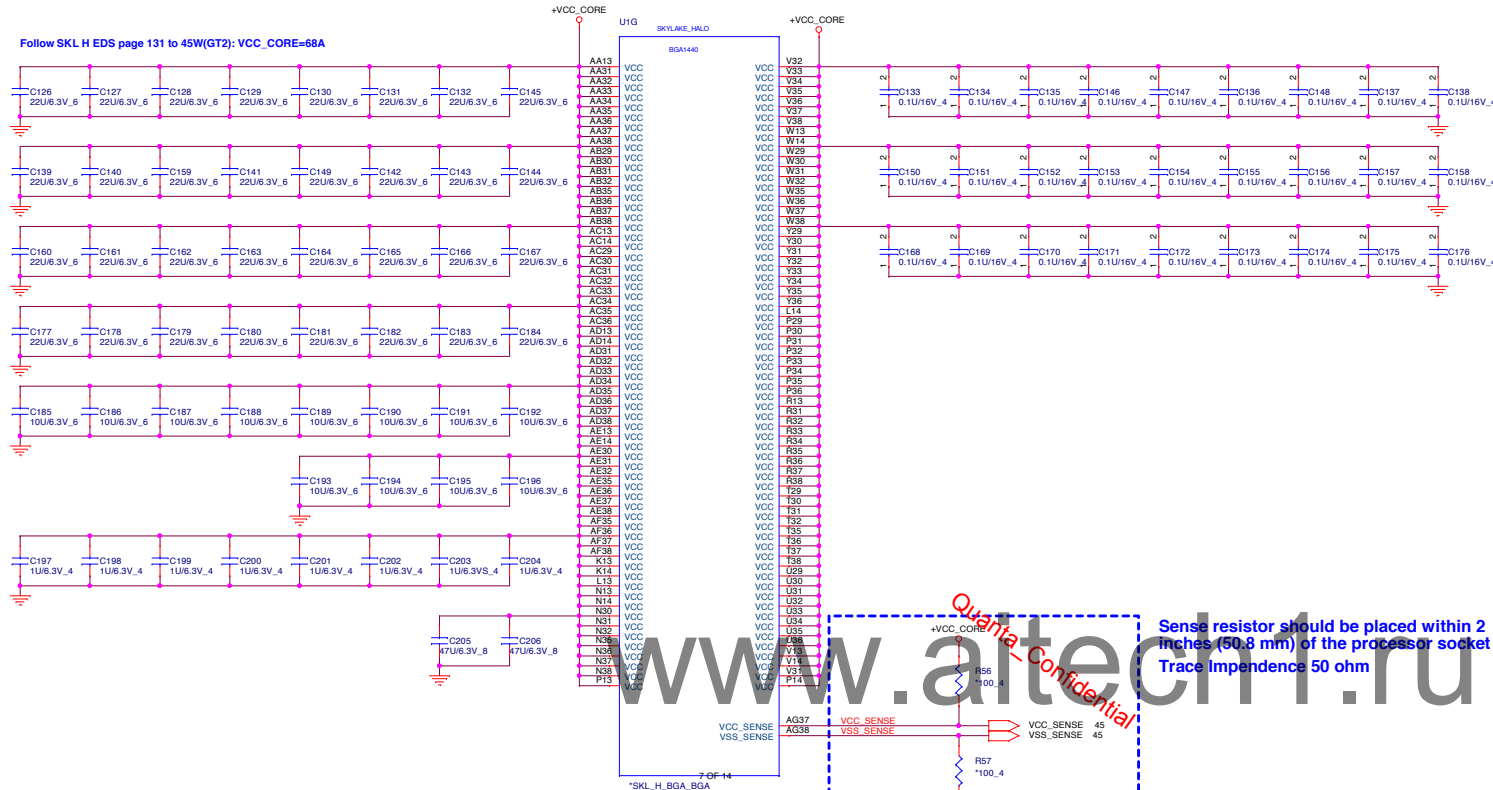
**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number SKL 4/7 (POWER)	Rev 1A
Date: Tuesday, May 31, 2016	Sheet 5 of 56	

Follow SKL H EDS page 135 45W: VDDQ=2.8A



Follow SKL H EDS page 131 to 45W(GT2): VCC\_CORE=68A



Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket  
Trace Impedance 50 ohm

+VCC\_CORE 45,46

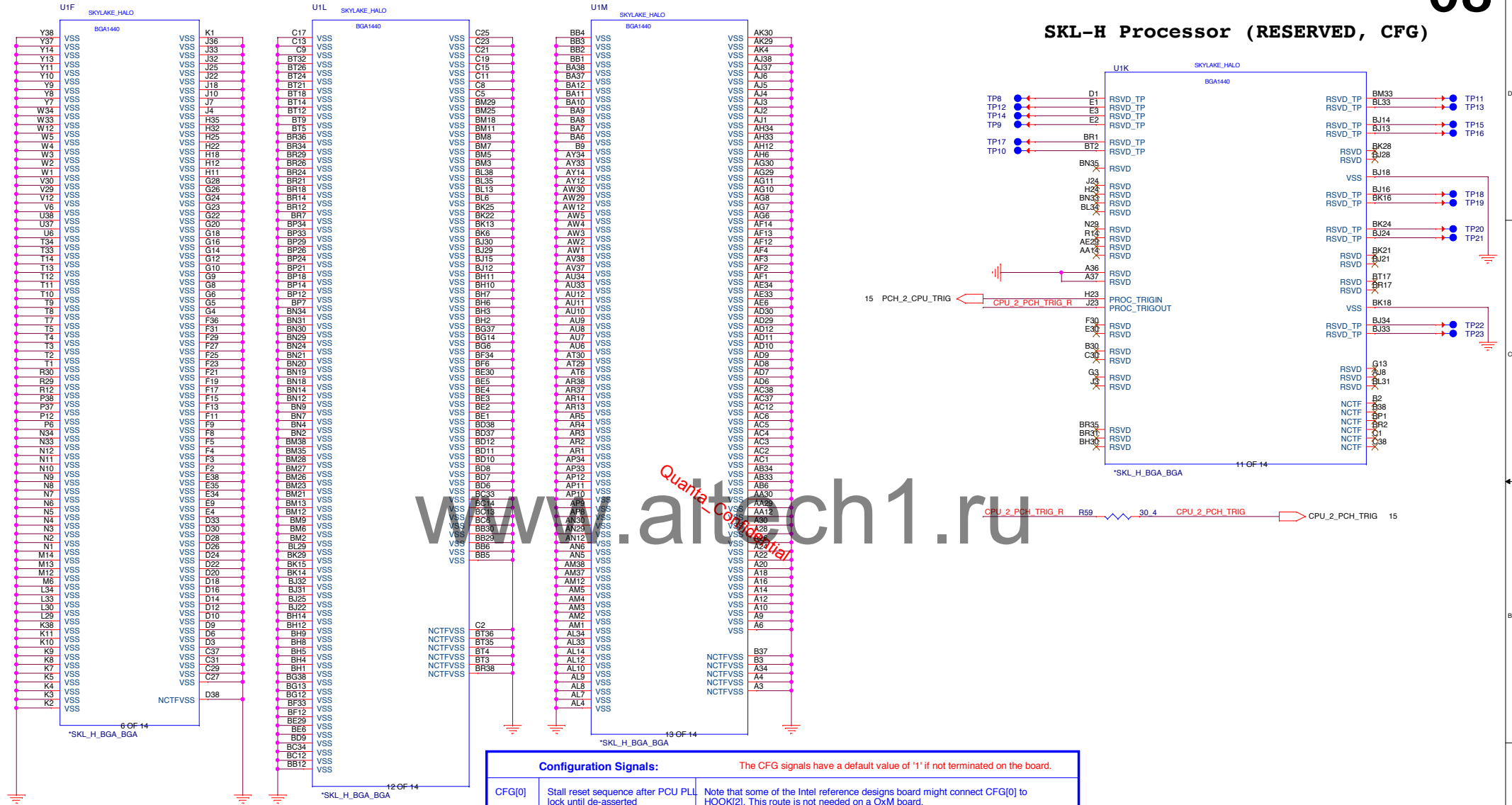


**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number SKL 6/7 (POWER&GND)	Rev 1A
Date: Tuesday, May 31, 2016	Sheet 7	of 56

SKL-HProcessor (GND)

SKL-H Processor (RESERVED, CFG)

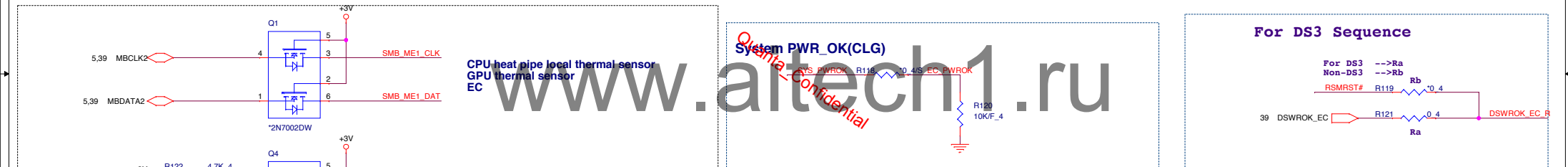


Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.	
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Note that some of the Intel reference designs board might connect CFG[0] to HOOK[2]. This route is not needed on a Oxm board.	
CFG[2]	PCI Express Static Lane Reversal	x1 = Normal operation x0 = Lane numbers reversed	
CFG[4]	eDP enable	x1 = Disabled x0 = Enabled	
CFG[6:5]	PCI Express Bifurcation	x00 = 1 x8 & 2 x4 PCI Express x01 = reserved	
		x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express	
CFG[7]	PEG defer training	x1 = PEG train follow RESETB de-asserted x0 = PEG wait for BIOS fro training	

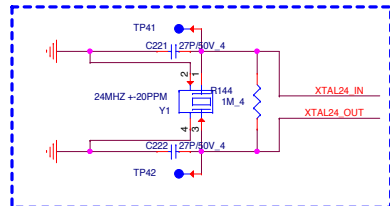


Quanta Confidential

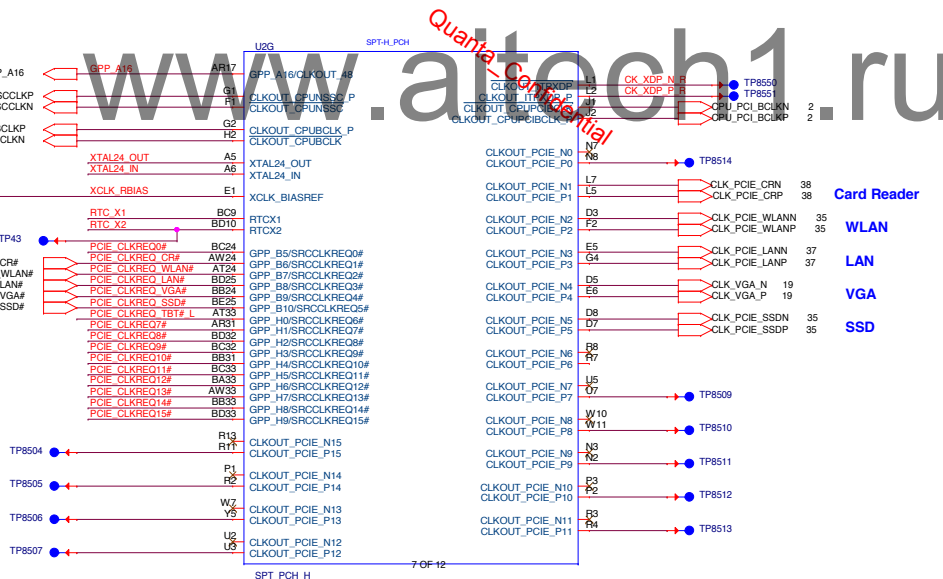
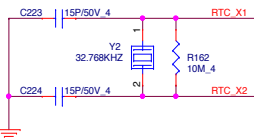








## RTC Clock 32.768KHz



```

-----
| GPIO35:
| SSD SATA IF => High
| SSD PCIE IF  => Low

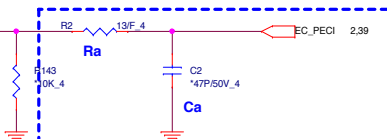
```

For SSD Det (SATA0A)

**BOM:SSD only**

SSD PCIE x4 (SATA0A) LANE

SSD PCIE x4 LANE



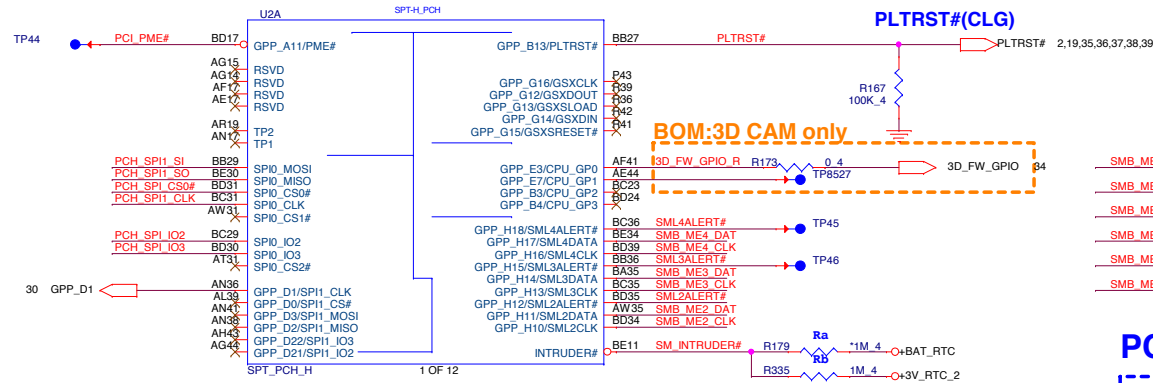
H\_PECI (50ohm)  
Trace Length: <0.5 inches  
Ra,Ca need placement close to PCH.

### Card Reader

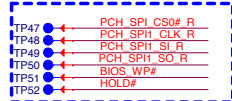
**BOM:DIS only**

**BOM:SSD only**

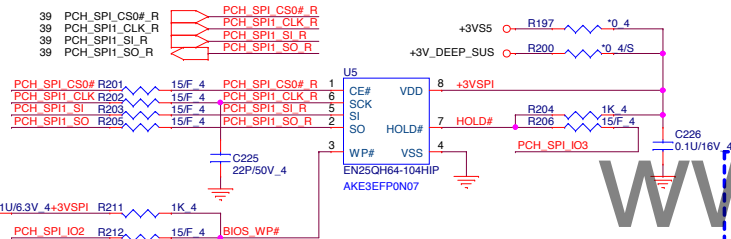
PCIE_CLKREQ0_WLAN#	R148		*10K 4
PCIE_CLKREQ0_LAN#	R149		*10K 4
PCIE_CLKREQ0_CH1#	R151		*10K 4
PCIE_CLKREQ0_VGA#	R152		*10K 4
PCIE_CLKREQ00#	R153		*10K 4
PCIE_CLKREQ0 SSD#	R154		*10K 4
PCIE_CLKREQ0 TB1# L	R155		*10K 4
PCIE_CLKREQ07#	R156		*10K 4
PCIE_CLKREQ08#	R157		*10K 4
PCIE_CLKREQ009#	R158		*10K 4
PCIE_CLKREQ010#	R159		*10K 4
PCIE_CLKREQ011#	R160		*10K 4
PCIE_CLKREQ012#	R161		*10K 4
PCIE_CLKREQ013#	R163		*10K 4
PCIE_CLKREQ014#	R164		*10K 4
PCIE_CLKREQ015#	R165		*10K 4



## PCH SPI ROM(CLG)

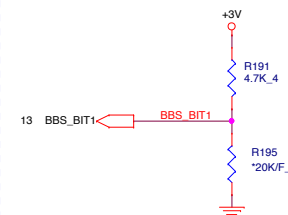


## Place to TOP

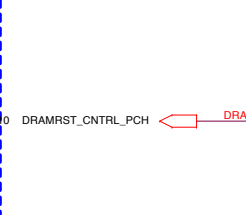


Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFPON07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE2EZNOQ00 (GD25B64CSIGR)
Socket		DFHS08FS023

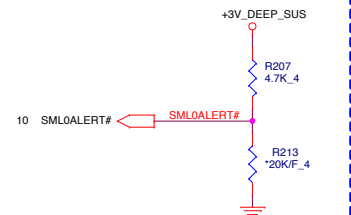
**NO REBOOT IF SAMPLED HIGH**  
HIGH: TOP SWAP ENABLED (CRB)  
LOW: Disable "No Reboot" mode. (Default)



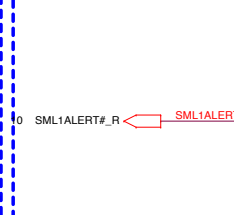
**ESPI/LPC SELECT STRAP**  
HIGH: ESPI is selected for EC.  
LOW: LPC is selected for EC. (Default)



**TLS CONFIDENTIALITY ENABLED**  
HIGH: T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)  
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

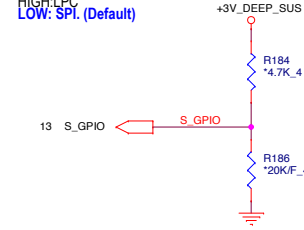


**RESERVED**  
This strap should sample LOW.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.

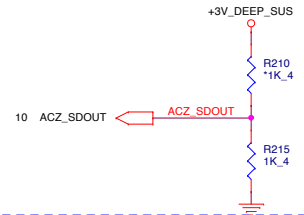


## PCH Strap Pin

**BOOT SELECT STRAP**  
HIGH: LPC  
LOW: SPI. (Default)

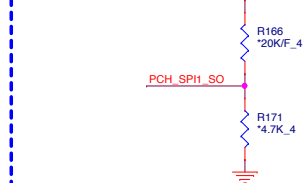


**TLS CONFIDENTIALITY ENABLED**  
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. (CRB)  
LOW: security measures defined in the Flash Descriptor. (Default)



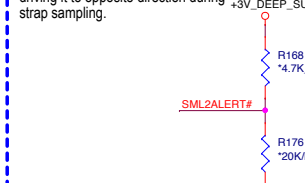
## RESERVED

This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



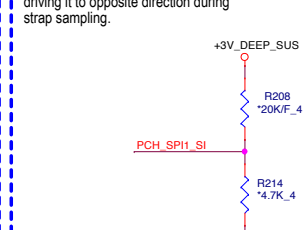
## ESPI FLASH SHARING MODE

HIGH: SLAVE ATTACHED FLASH SHARING  
LOW: 0: MASTER ATTACHED FLASH SHARING  
This strap should sample LOW.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.

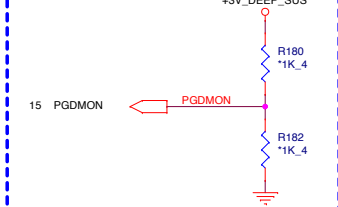


## RESERVED

This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.

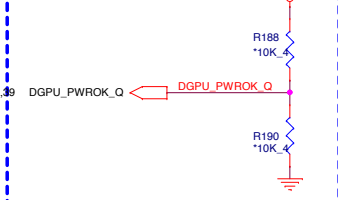


DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



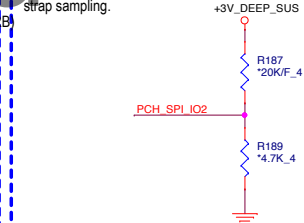
## DFX TEST MODE

XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



## RESERVED

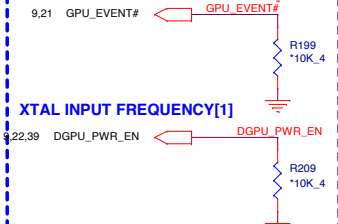
This strap should sample HIGH.  
There should NOT be any on-board device driving it to opposite direction during strap sampling.



## RING OSCILLATOR BYPASS



XTAL INPUT FREQUENCY[0]



XTAL INPUT FREQUENCY[1]

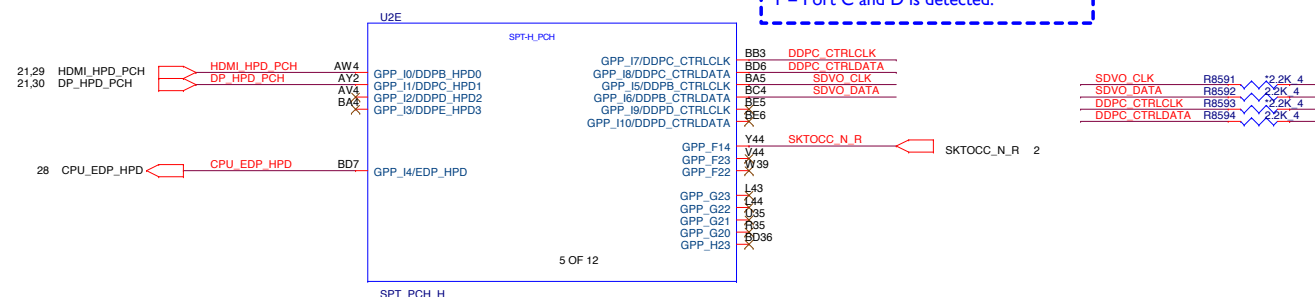


**PROJECT : G38A**  
Quanta Computer Inc.

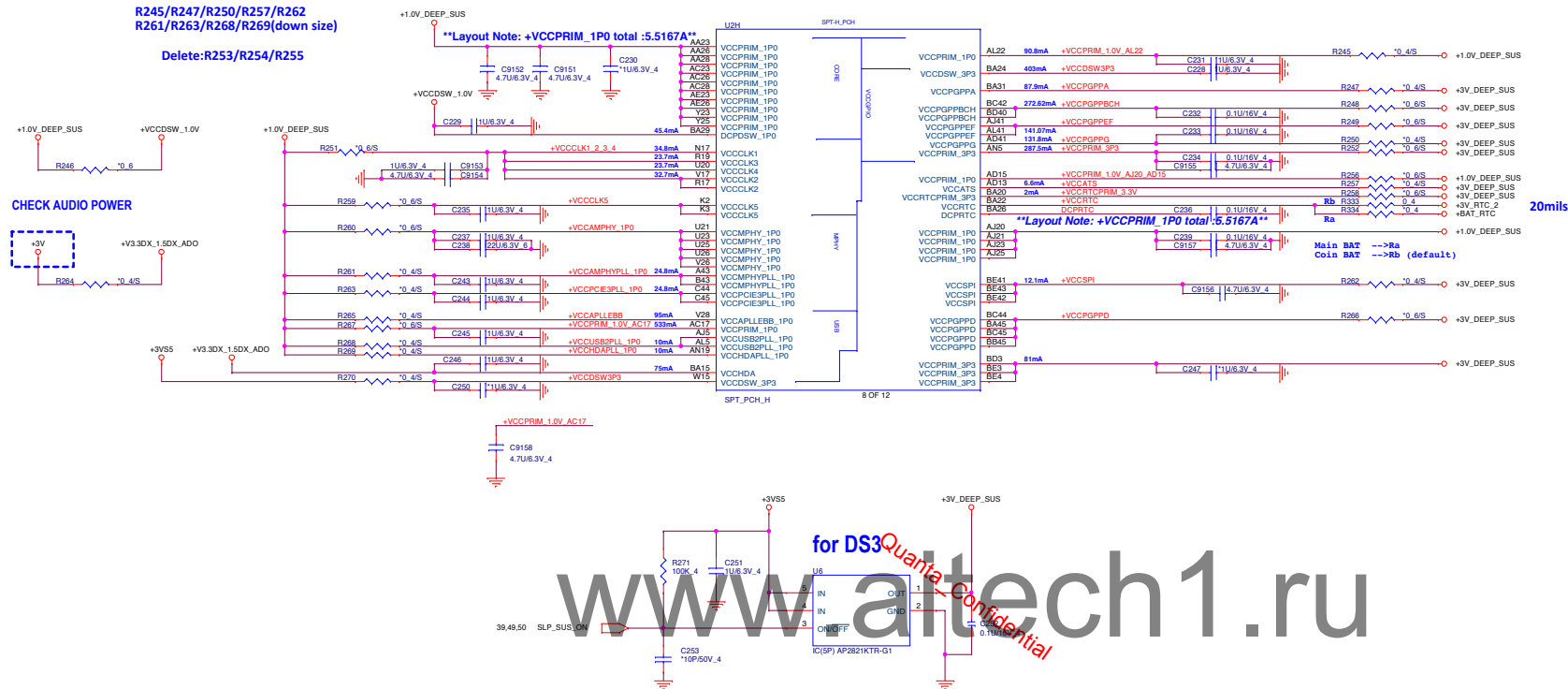
Size	Document Number	Rev
Custom	PCH 4/7 (GPIOMISC)	1A
Date: Tuesday, May 31, 2016	Sheet 12 of 56	

Board ID

Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3]		BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H	00 Reserved	ID4 Reserve	ID3 0 NVidia 1 AMD	00 15" P SKL H 01 17" P SKL H 10 17" SP SKL H 11 Reserved	0 : UMA 1 : DIS

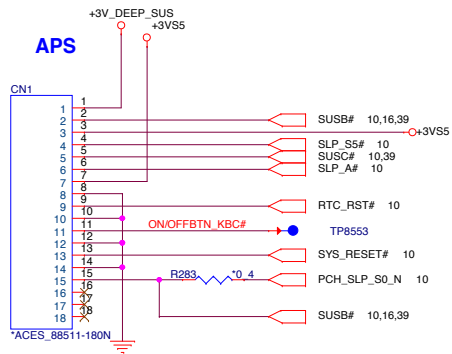


- This signal has a weak internal pull-down.
- 0 = Port C and D is not detected.
- 1 = Port C and D is detected.



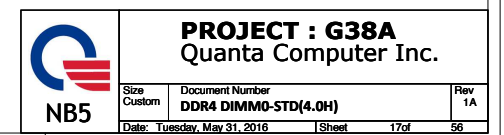


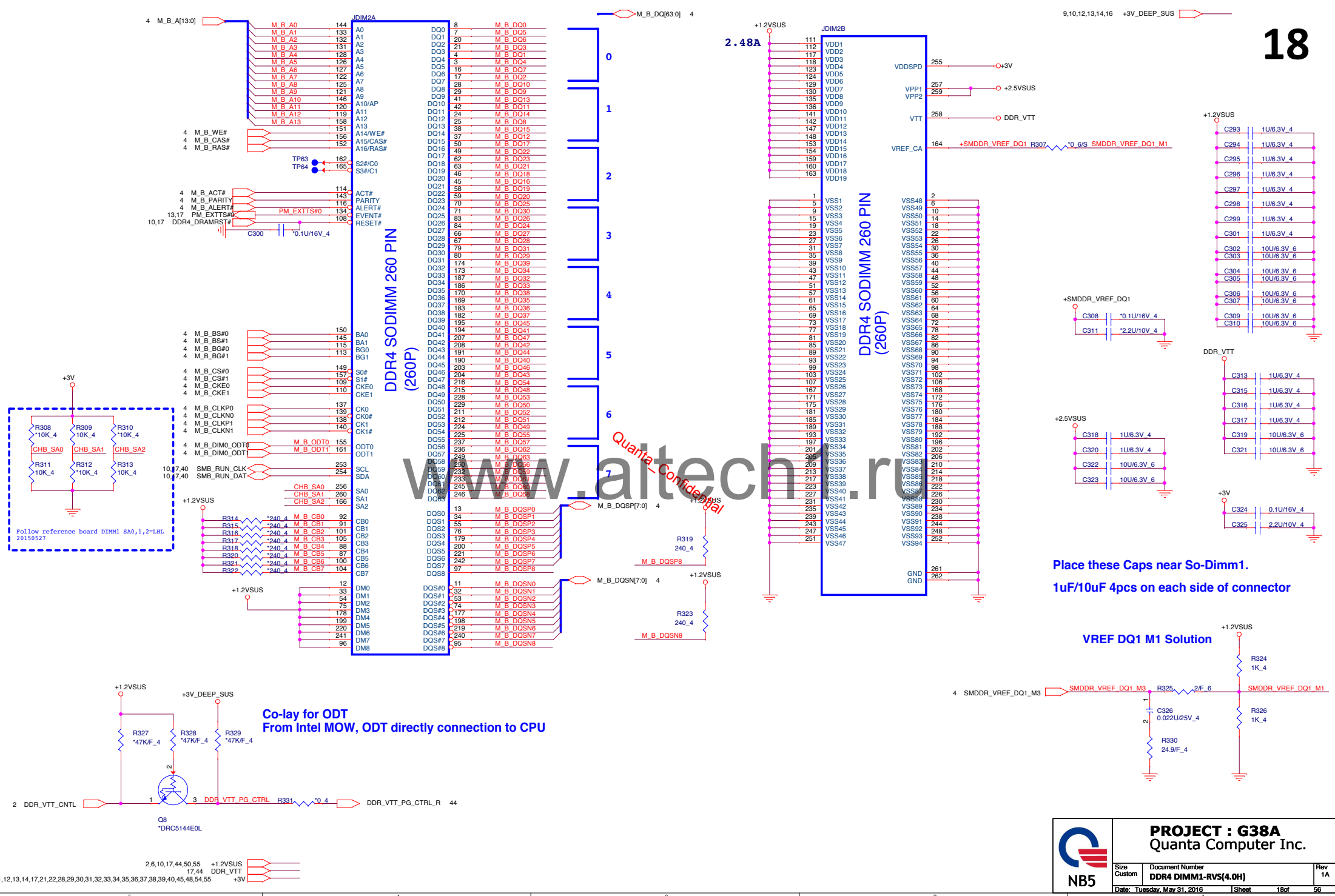
www.altech1.ru

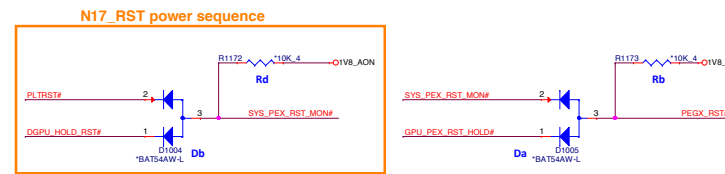


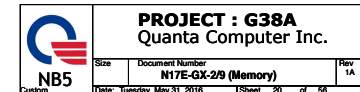
9,10,12,13,14,18 +3V\_DEEP\_SUS





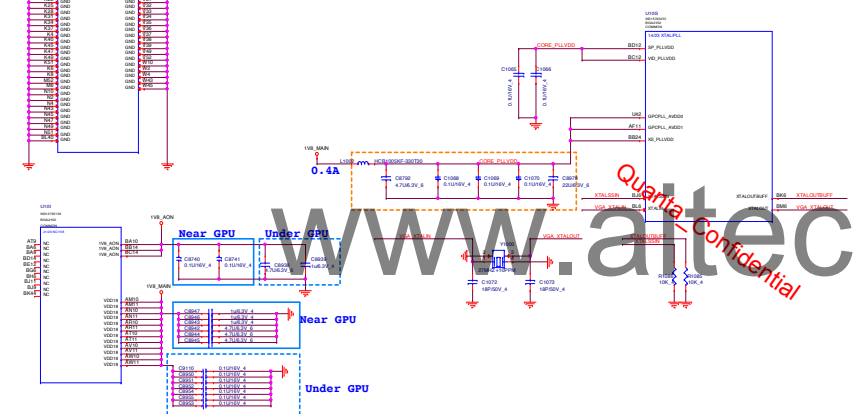
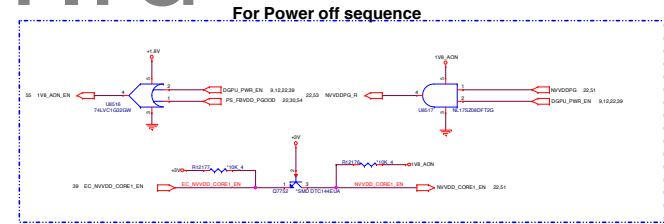
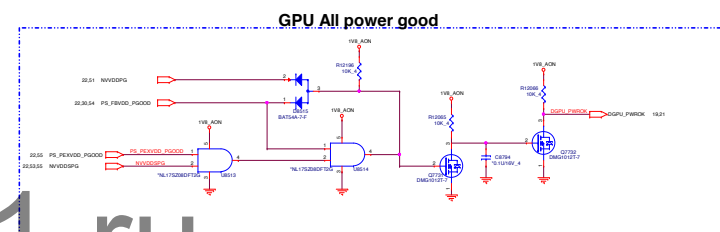
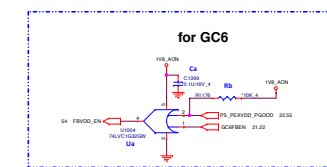
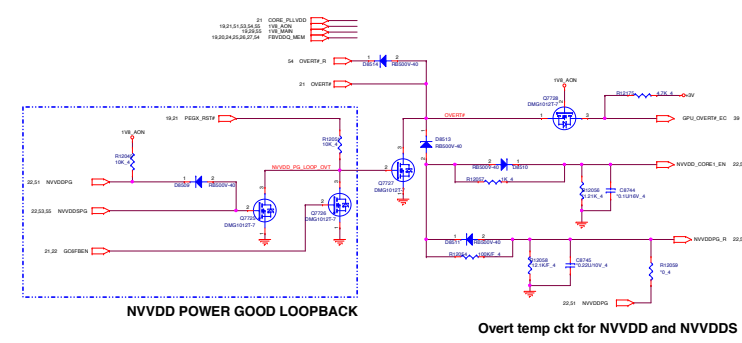
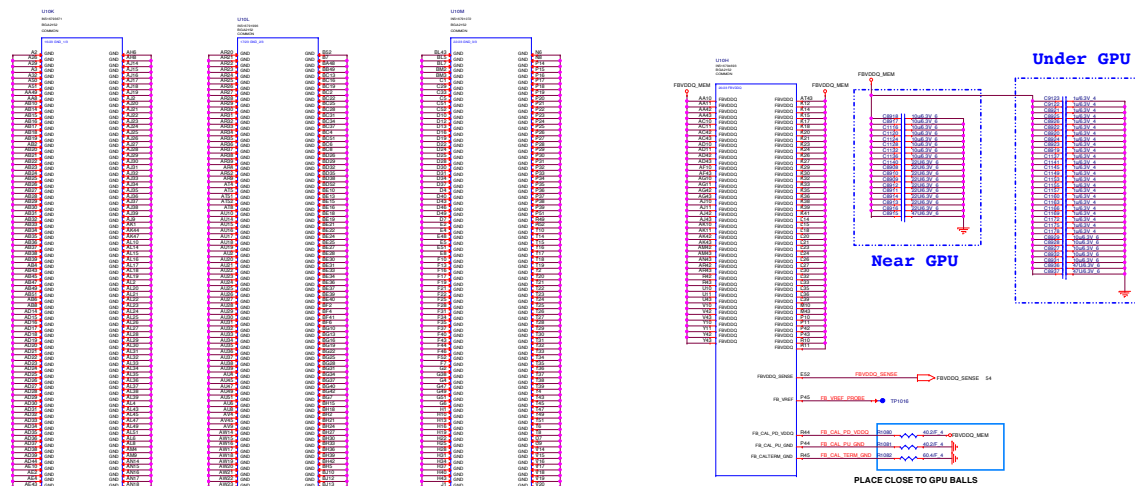




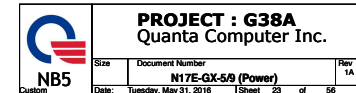




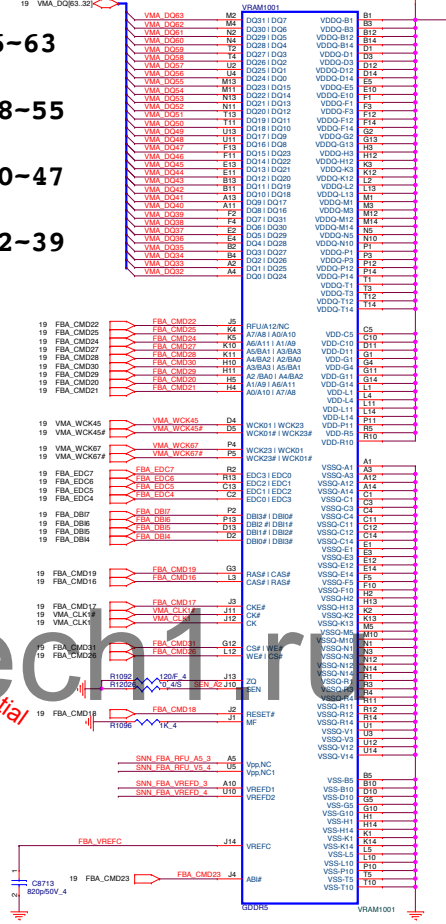








FBVDDQ\_MEM



GB3-256		Channel 0 3_1	GB3-256	Channel 1 32.63
CM00	CAS*	CM016	CAS*	
CM01	CKE	CM017	CKE	
CM02	RST*	CM018	RST*	
CM03	RA5*	CM019	RA5*	
CM04	A1_A9	CM020	A1_A9	
CM05	A0_A10	CM021	A0_A10	
CM06	A12_RFU	CM022	A12_RFU	
CM07	AB1*	CM023	AB1*	
CM08	A6_A11	CM024	A6_A11	
CM09	A7_A8	CM025	A7_A8	
CM010	WE*	CM026	WE*	
CM011	A5_BA1	CM027	A5_BA1	
CM012	A4_BA2	CM028	A4_BA2	
CM013	A2_BA0	CM029	A2_BA0	
CM014	A3_BA3	CM030	A3_BA3	
CM015	CS*	CM031	CS*	
GB3-256 Channel 0 B 1				
CM032	Hot used			
CM033	Hot used			
CM034	DEBUG0			
CM035	DEBUG1			

Notes:

1. GPU debug pins, not connected to DRAM. See section 7.1-13.

Channel 1  
<0-31>Channel 0  
<0-31>

MF=1 mirrored

MF=0 Non-mirrored



QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

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QD24-31

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QD48-55

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QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

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QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

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QD0-7

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QD48-55

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QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

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QD48-55

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QD16-23

QD8-15

QD0-7

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QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-15

QD0-7

QD56-63

QD48-55

QD40-47

QD32-39

QD24-31

QD16-23

QD8-

Channel 0  
<0-31>

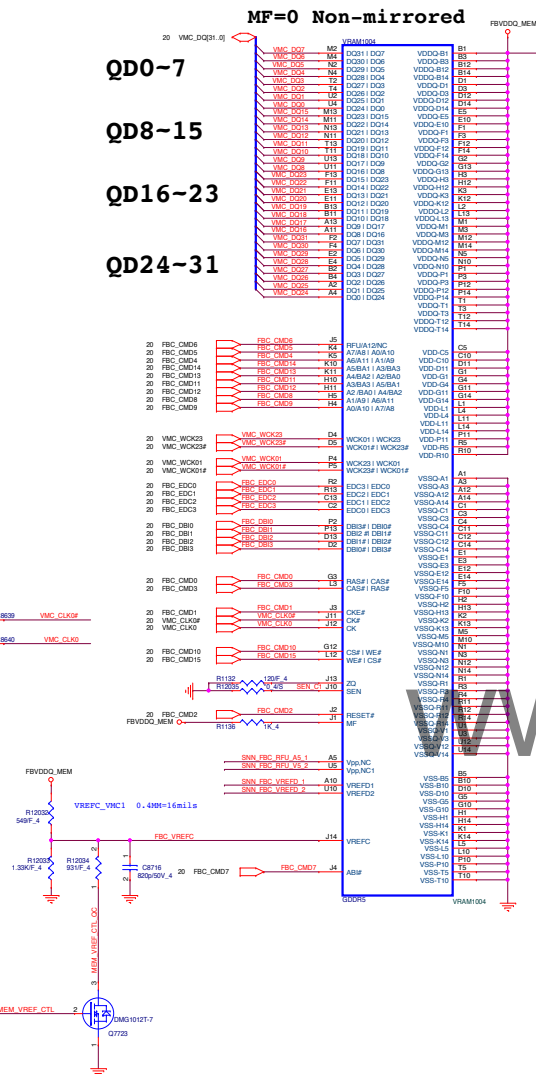
MF=0 Non-mirrored

QD0-7

QD8-15

QD16-23

QD24-31

Channel 1  
<0-31>

MF=0 Non-mirrored

QD56-63

QD48-55

QD40-47

QD32-39



Table 7-5. GDDR5 Mode F Mapping

GB3-256	Channel 0 0..31	GB3-256	Channel 1 32..63
CMD0	CAS*	CMD16	CAS*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RAS*	CMD19	RAS*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	AB*	CMD23	AB*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	C5*	CMD31	C5*
GB3-256 Channel 0 B 1			
CMD32	Hot used		
CMD33	Hot used		
CMD34	DEBUG*		
CMD35	DEBUG*		

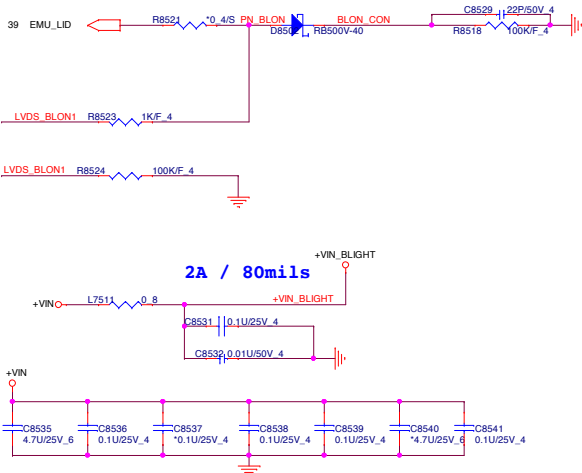
Notes:

1. GPU debug pins; not connected to DRAM. See section 7.1.13.

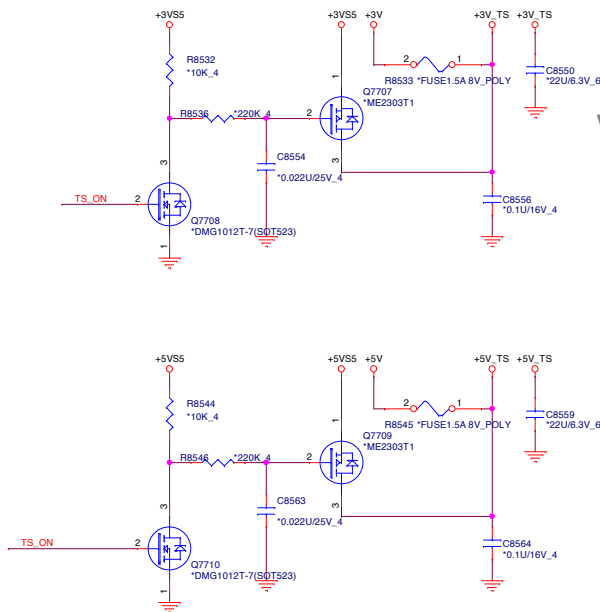




# LID Switch



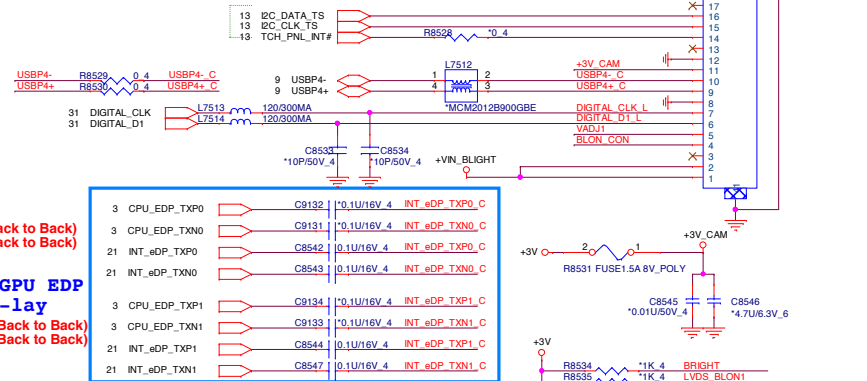
# Reserve for Touch screen



# eDP Conn.

MB	TS (V/F: I2C)
+3V_TS	VDD33
I2C_DATA_TS	SDA
I2C_CLK_TS	SCL
TCH_PNL_RST#_EC	EXRESETN
TCH_PNL_INT#	ATTN
TS_ON	Report_Switch
GND	GND

for NVSR(Gsync)



C9132/C8542(Back to Back)  
C9131/C8543(Back to Back)

# CPU/GPU EDP co-layer

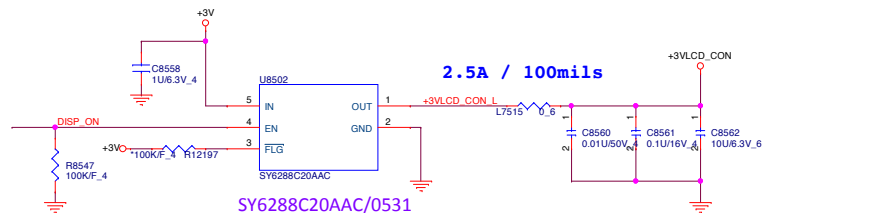
C9134/C8544(Back to Back)  
C9133/C8547(Back to Back)

# CPU/GPU EDP co-layer

C9136/C8553(Back to Back)  
C9135/C8545(Back to Back)

# CPU/GPU EDP co-layer

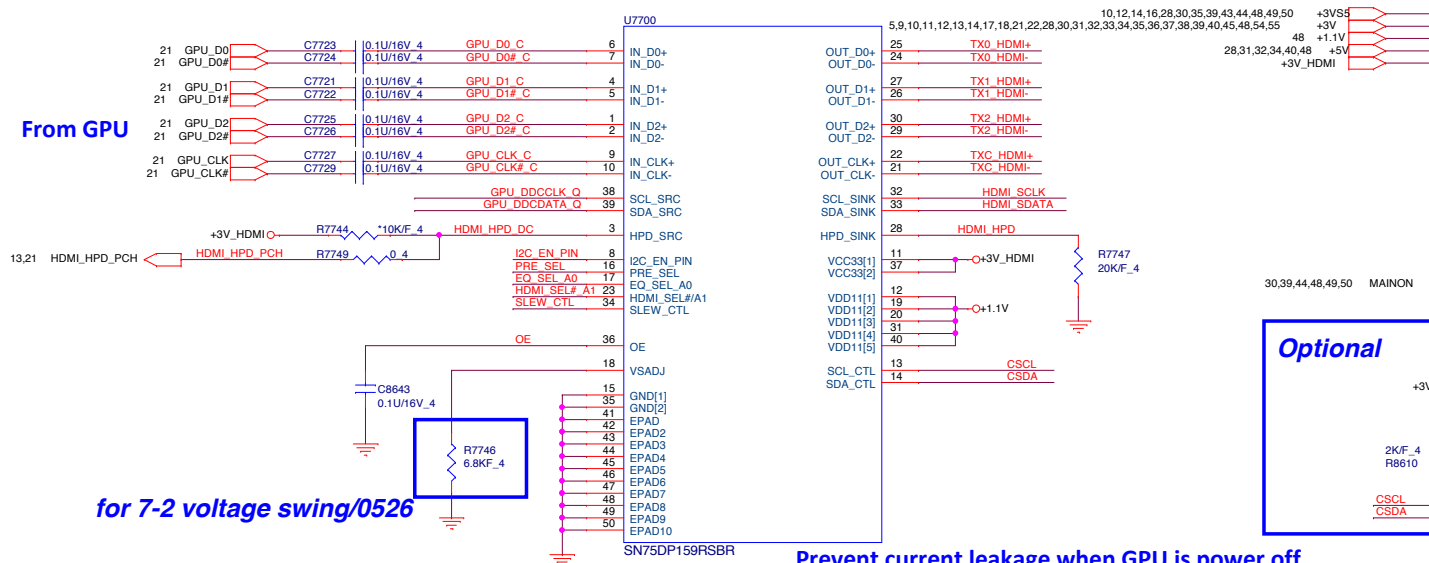
C9136/C8553(Back to Back)  
C9135/C8545(Back to Back)



5,9,10,11,12,13,14,17,18,21,22,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55  
5,10,21,33,35,39,40,42,43,51 +3VPCU  
29,31,32,34,40,48 +5V  
40,41,42,43,44,45,46,47,48,49,50,51,54 +VIN

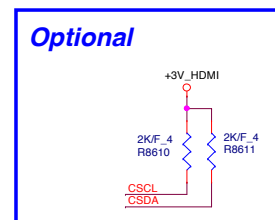


## From GPU

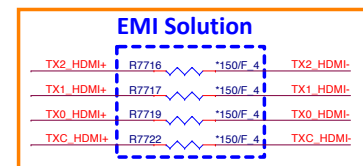


**for 7-2 voltage swing/0526**

Prevent current leakage when GPU is power off  
add R12317/R1231 is for HDMI verify



**Optional**



## EMI Solution

**SN75DP159RSBR strap**

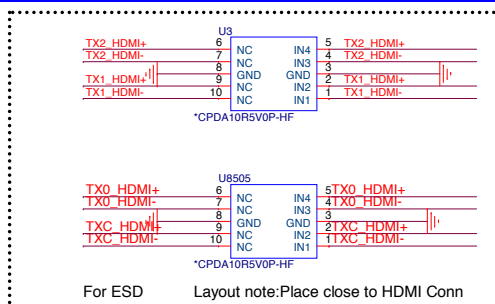
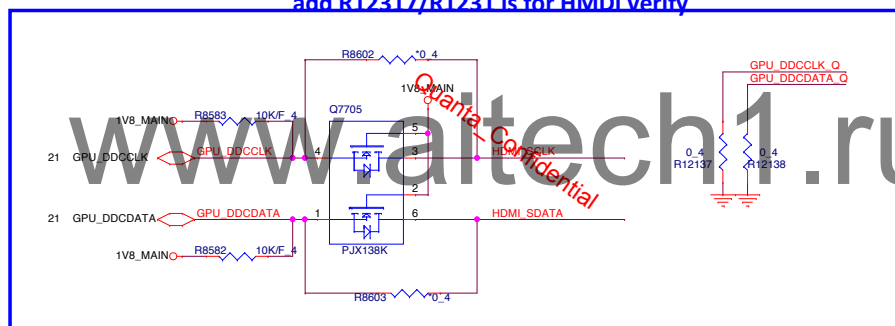
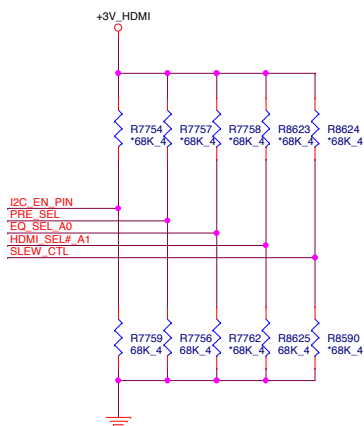
I2C\_EN/PIN = High; puts device into I2C control mode  
I2C\_EN/PIN = Low; puts device into pin strap mode

De-emphasis pin strap when I2C\_EN/PIN = Low.  
PRE\_SEL = L: - 2 dB de-emphasis  
PRE\_SEL = No Connect: 0 dB  
PRE\_SEL = H: Reserved

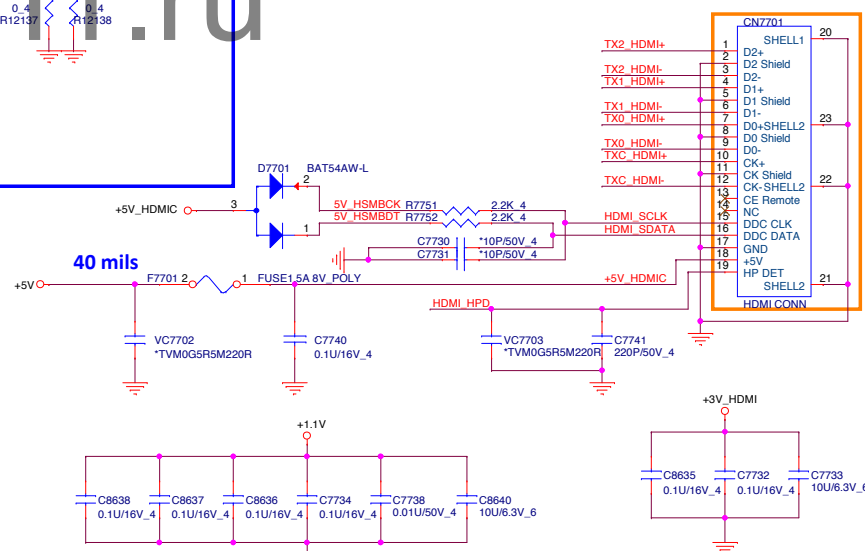
Input Receive Equalization pin strap when I2C\_EN/PIN = Low  
EQ\_SEL = L: Fixed EQ at 7.5 dB  
EQ\_SEL = No Connect: Adaptive EQ  
EQ\_SEL = H: Fixed at 14 dB

HDMI\_SEL when I2C\_EN/PIN = Low  
HDMI\_SEL = High: Device configured for DVI  
HDMI\_SEL = Low: Device configured for HDMI

Slew rate control when I2C\_EN/PIN = Low.  
SLEW\_CTL = H, fastest data\_rate  
SLEW\_CTL = L, 5 ps slow  
SLEW\_CTL = No Connect, 10 ps slow



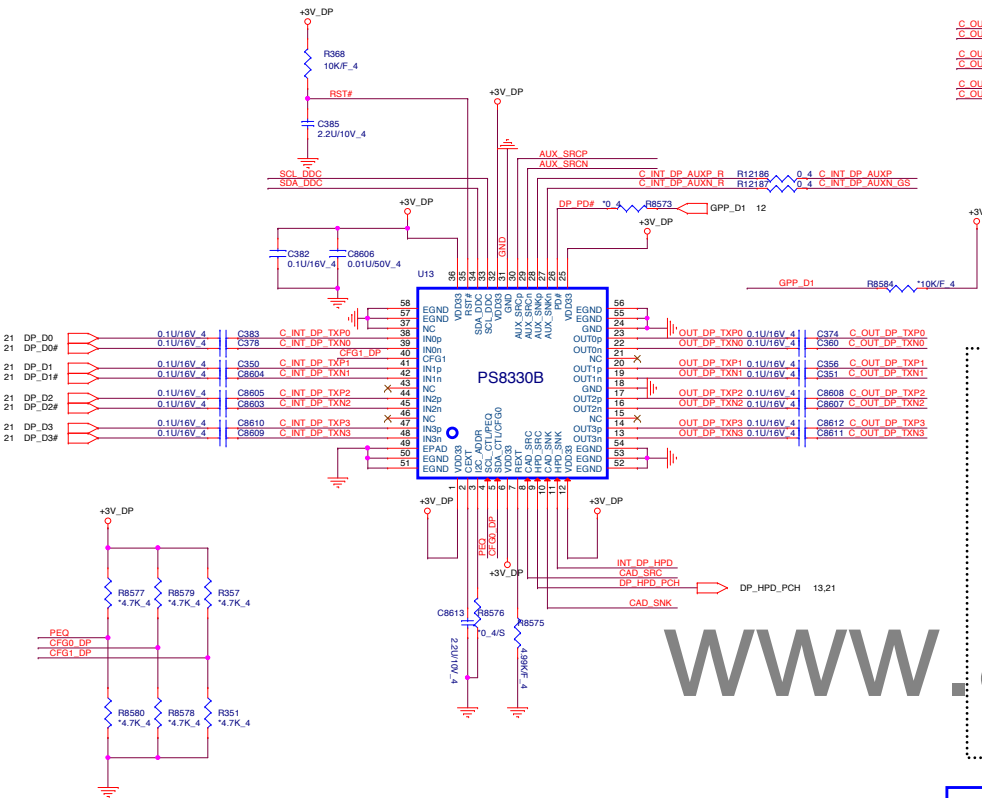
For ESD      Layout note:Place close to HDMI Conn

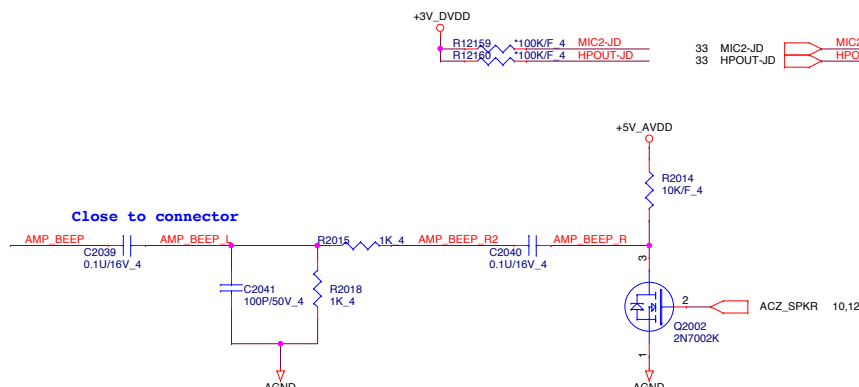
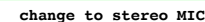
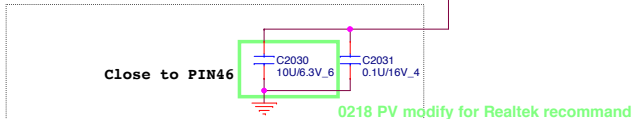


**PROJECT : G38A**  
Quanta Computer Inc.

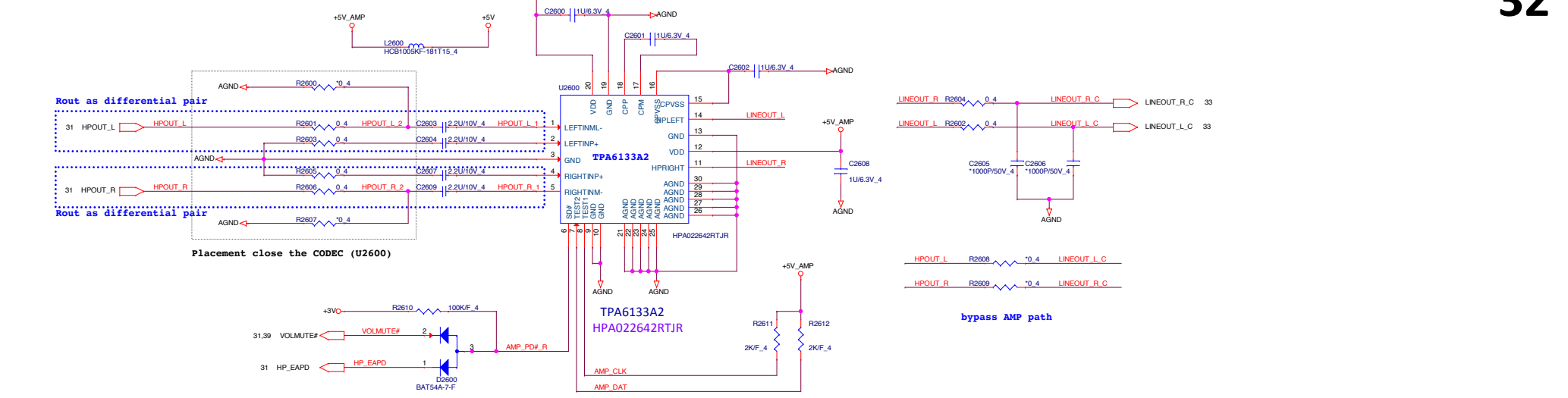
Size Custom	Document Number <b>HDMI/HDMI REDRIVER</b>	Rev 1A
Date: Tuesday, May 31, 2016	Sheet 29 of	56

5V 28,29,31,32,34,40,48  
3V 5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55

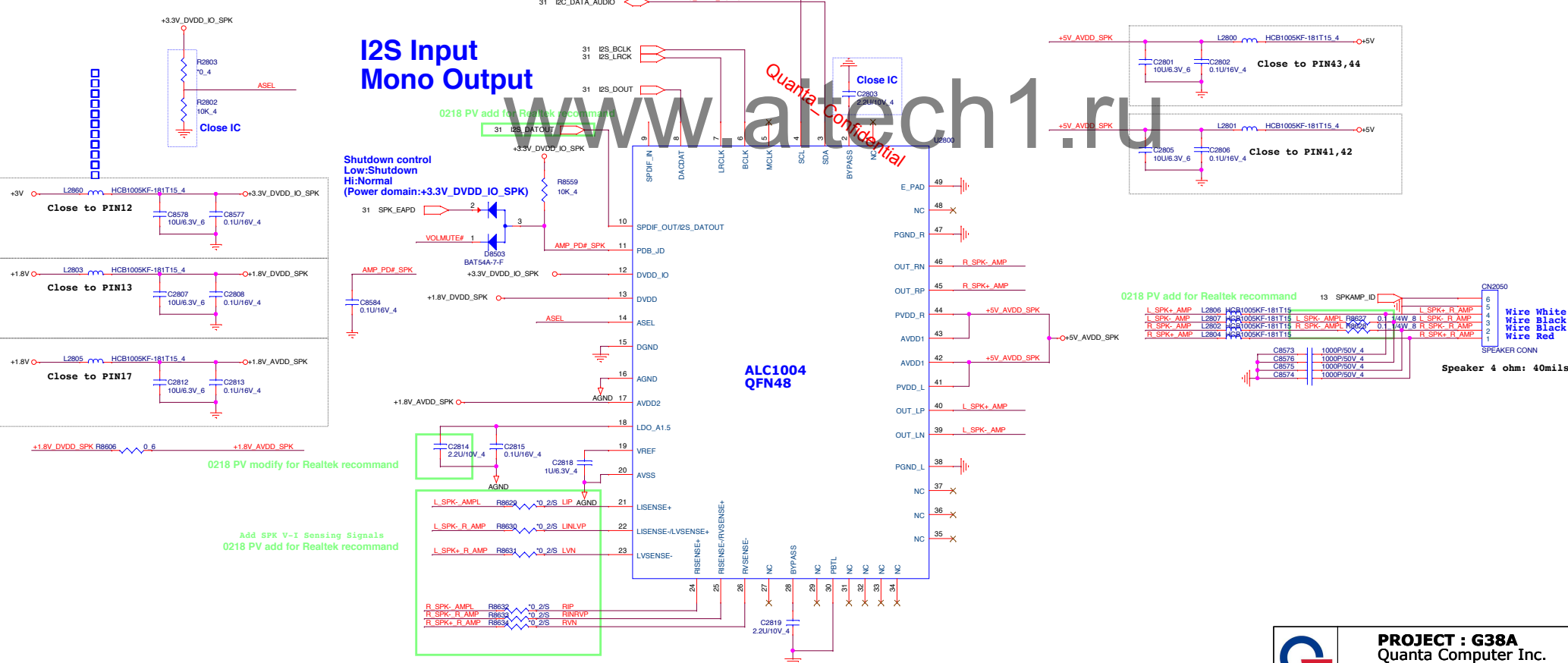


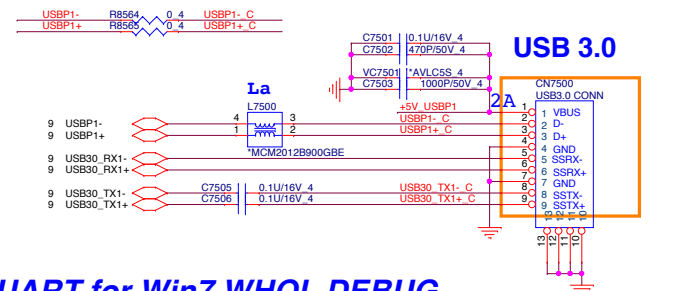
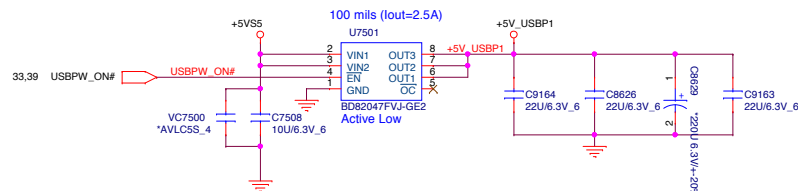


Head Phone out AMPLIFIER

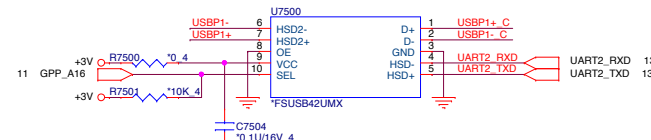


SPEAKER AUDIO AMPLIFIER



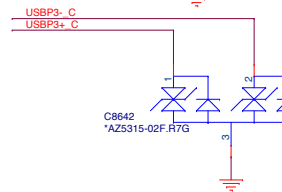
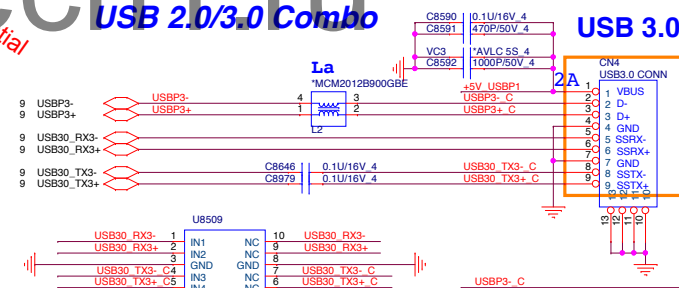


## UART for Win7 WHQL DEBUG

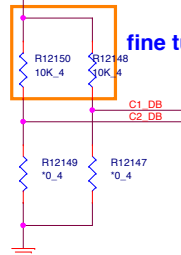


Place Back to Back La

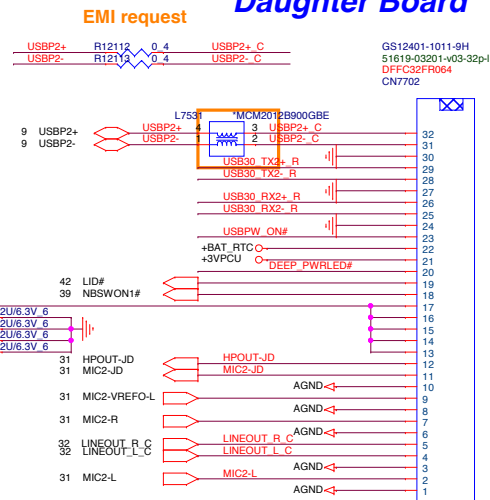
**USB 2.0/3.0 Combo**



S

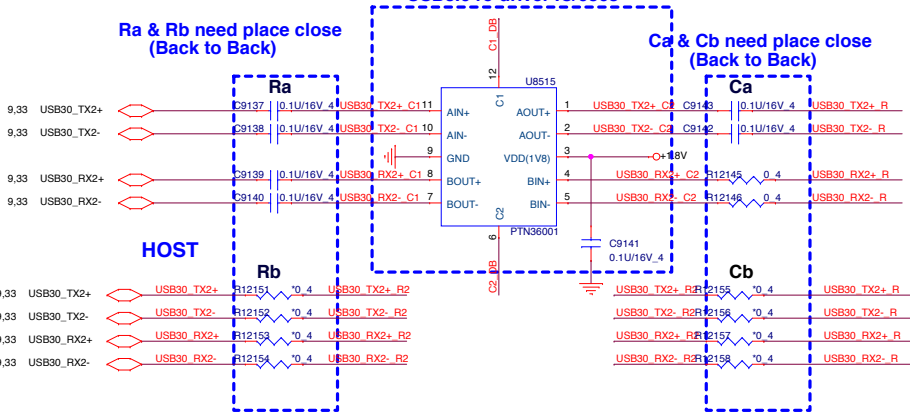


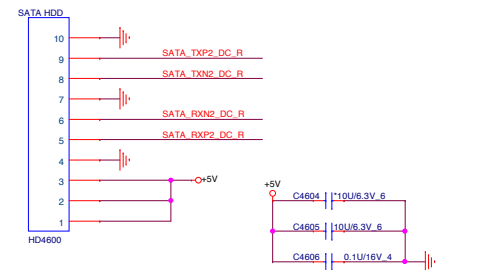
## ***Daughter Board***



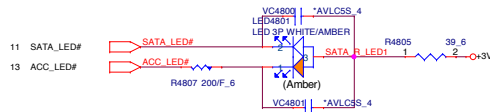
change to stereo MIC/0308

## USB3.0 re-driver IC/0308

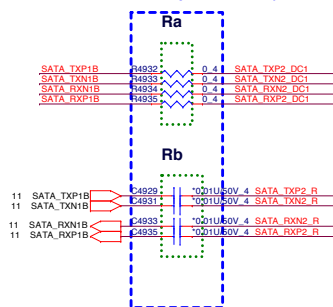




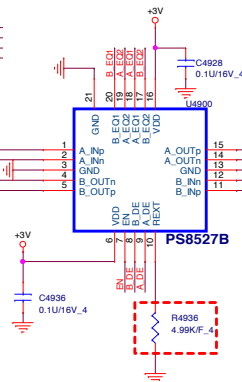
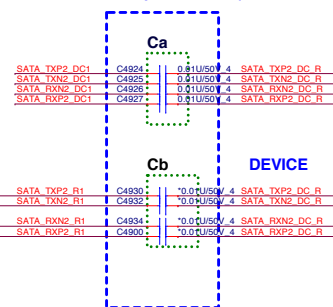
## SATA LED



Ra &amp; Rb need place close (Back to Back)



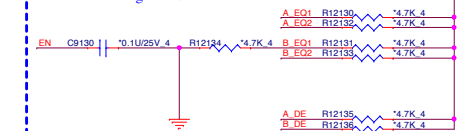
Ca &amp; Cb need place close (Back to Back)

SATA re-driver IC  
stuff Rb,Cb , unstuff Ra,Caunstuff SATA re-driver IC  
stuff Ra,Ca , unstuff Rb,Cb

Equalization level setting for Channel x(x=A/B), internally tied to VDD/2 (default:12.2dB)  
 $[x\_EQ2, x\_EQ1] =$   
 L/L: for channel loss up to 7.4dB  
 L/H: for channel loss up to 14.4dB  
 H/L: for channel loss up to 11.2dB  
 H/H: for channel loss up to 5dB

De-emphasis level setting for Channel x(x=A/B), internally tied to VDD/2(Default=3.5dB)  
 $[x\_DE] =$   
 L: 0 dB  
 H: -6dB

Reference design "DNI"



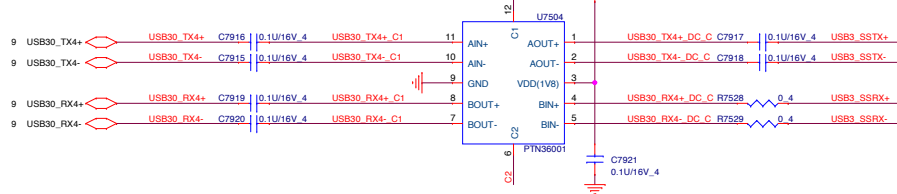
FAE suggest A-SMT use default setting (DNI)

Quanta Confidential

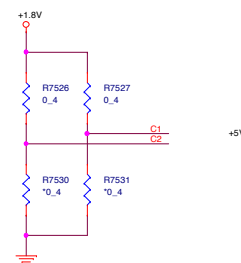
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## 3D CAMERA

HOST



USB3.0 re-driver IC



3D Camera Conn.

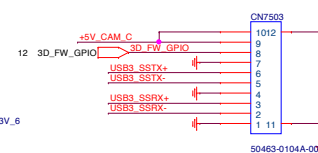
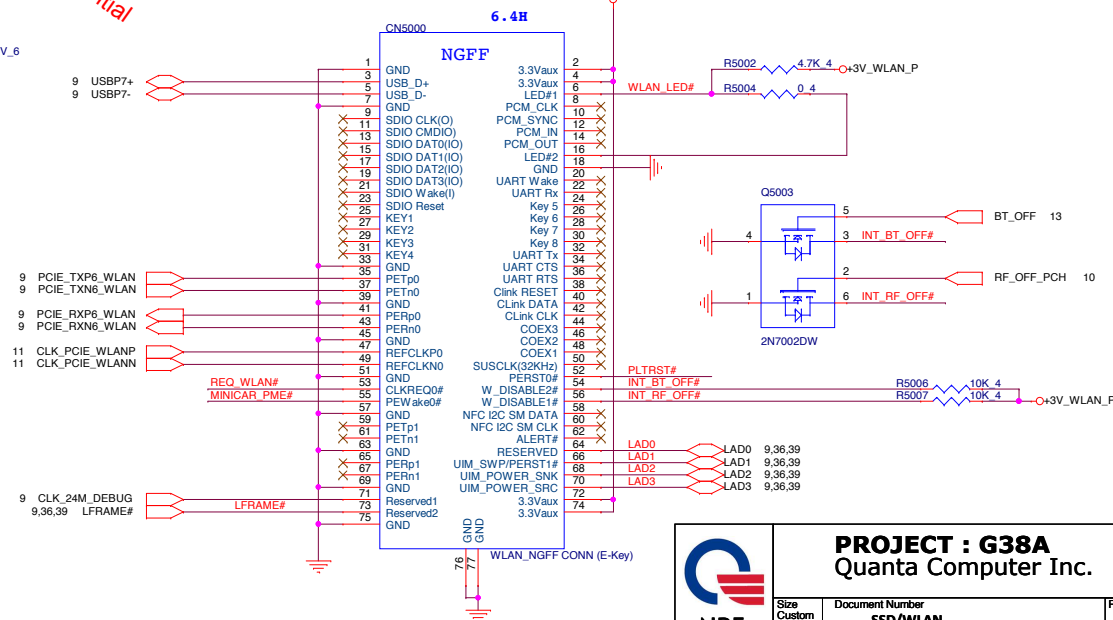
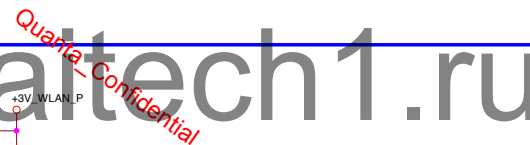
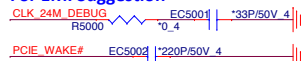


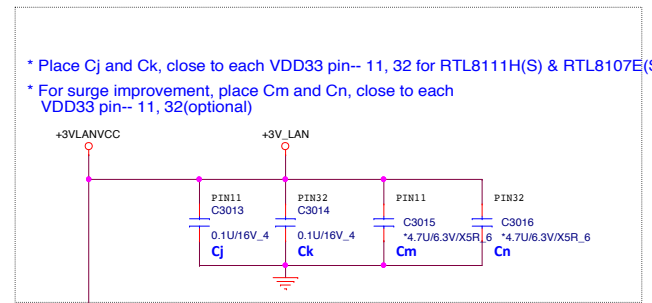
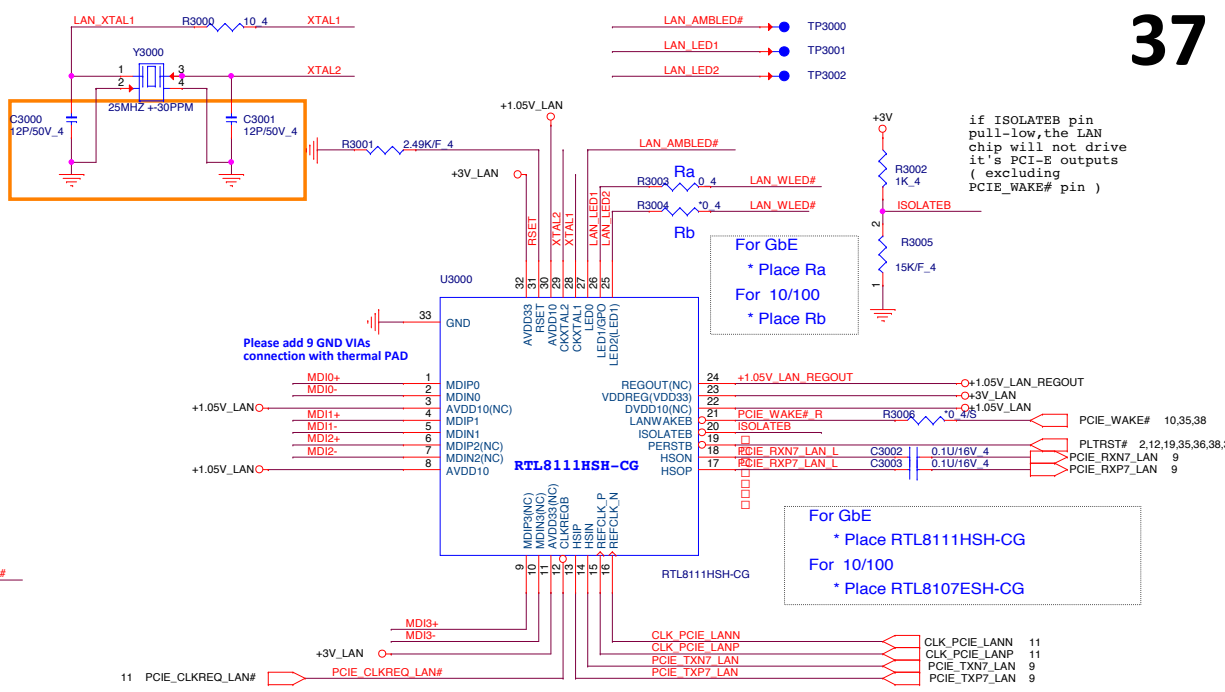
Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel B		
			EQ[1]	DE[2]	OS[3]
H	Long	H	9 dB	-5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	-3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

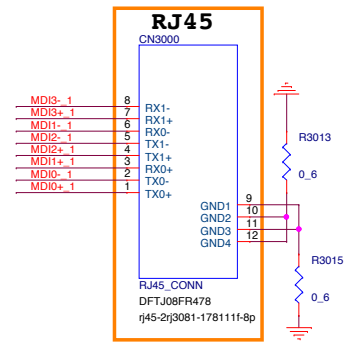
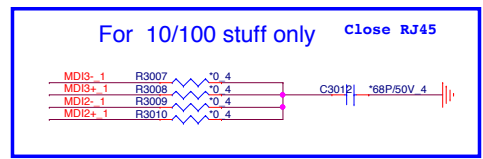
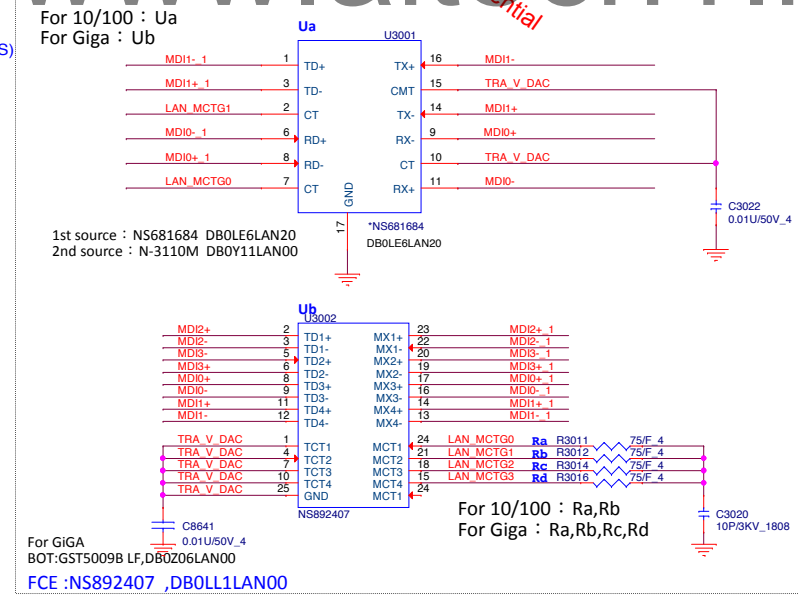




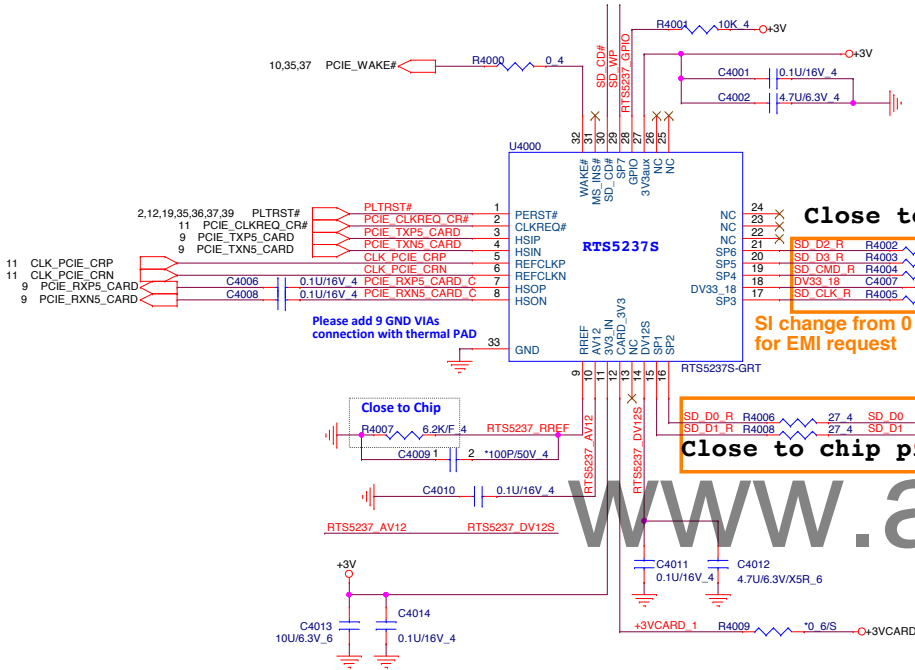




For 10/100 : Ua

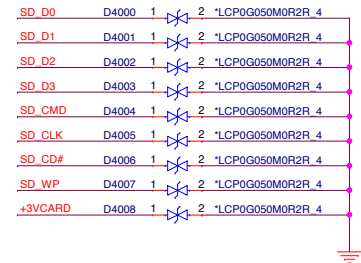
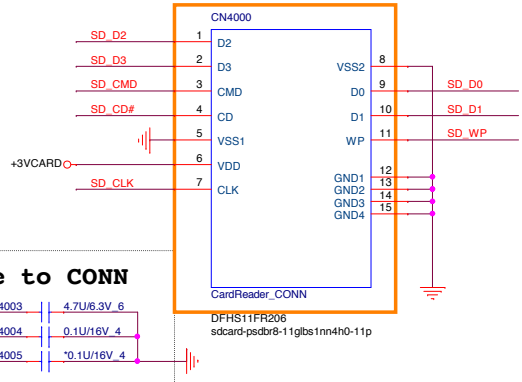


5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,39,40,45,48,54,55 +3V

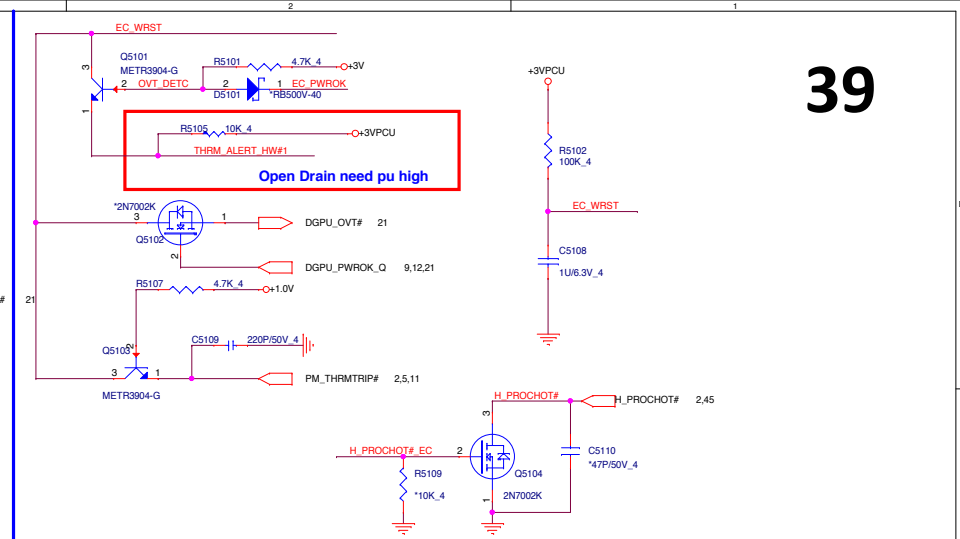
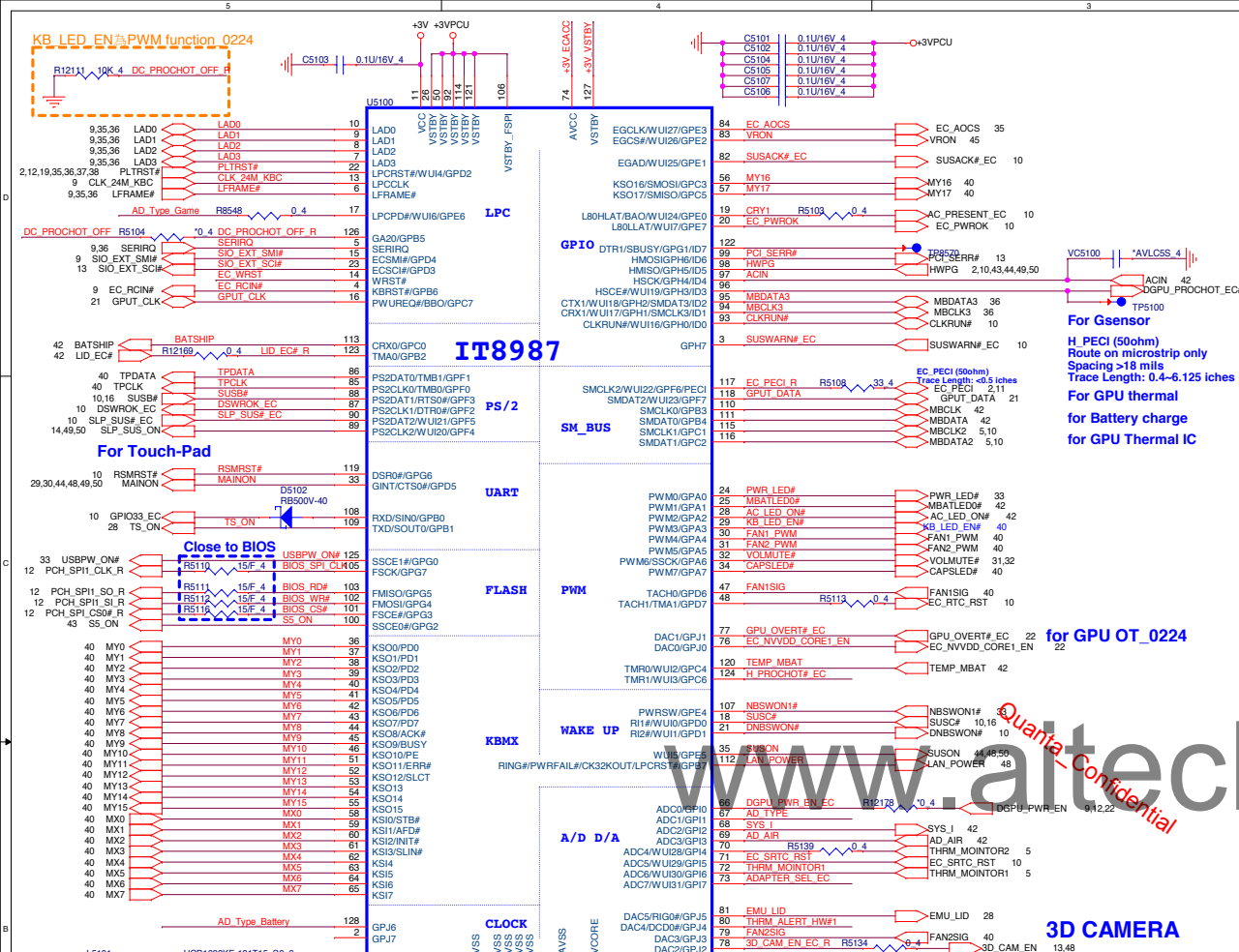


SP1	SD D1	MS D1
SP2	SD D0	MS D0
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD WP	MS BS

Share Pin  
SD / MMC



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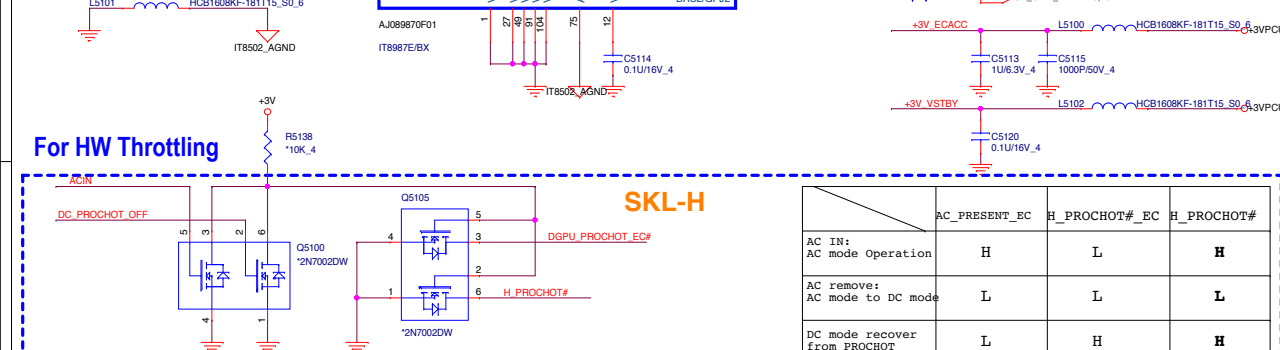
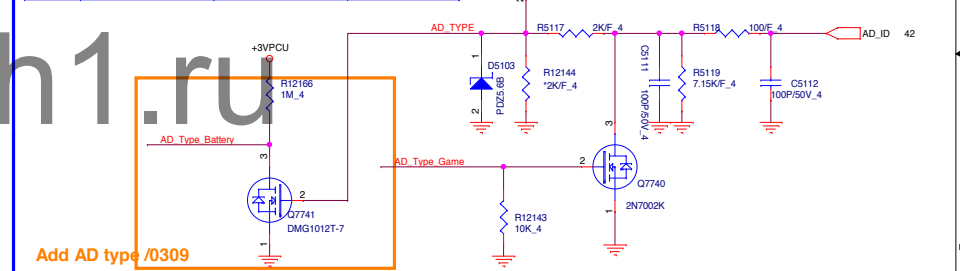


### Adapter select for EC

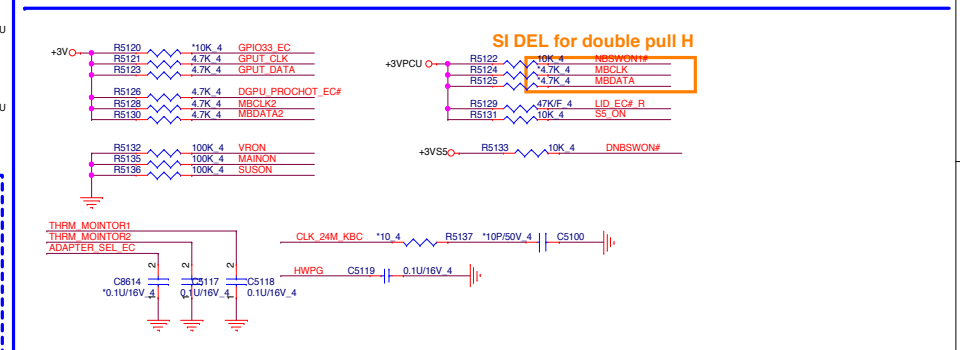
	Ra	Rb	ADAPTER_SEL_EC
200W	10K(CS31002FB26)	100K(CS41002FB28)	3V
230W	10K(CS31002FB26)	2.2K(CS22202JB18)	0.59V
330W	NC	10K(CS31002FB26)	0V

### adapter Type check

D5100  
1S355      Change to 1S355 as Current loss



	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	<b>H</b>	<b>L</b>	<b>H</b>
AC remove: AC mode to DC mode	<b>L</b>	<b>L</b>	<b>L</b>
DC mode recover from PROCHOT	<b>L</b>	<b>H</b>	<b>H</b>

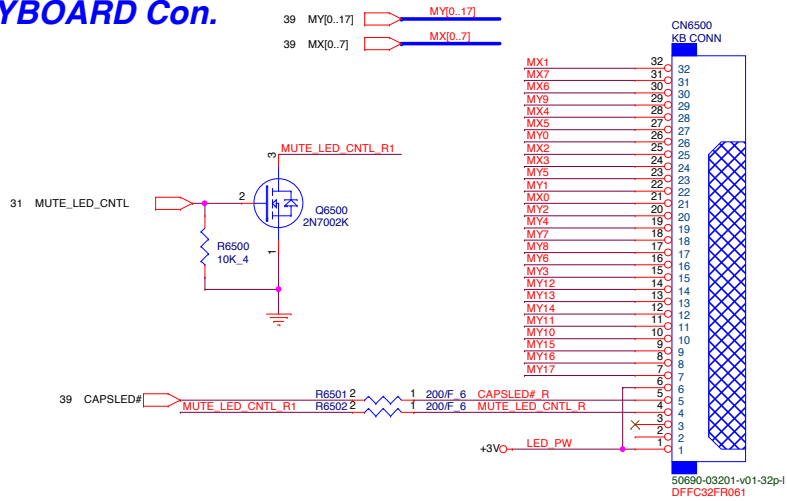


5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,40,45,48,54,55  
5,10,21,33,35,40,42,43,51

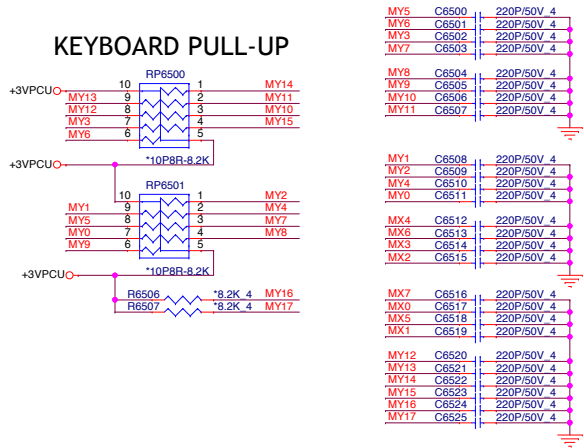
+3V  
+3VPCU

**Need to CL OSE to EC pin**

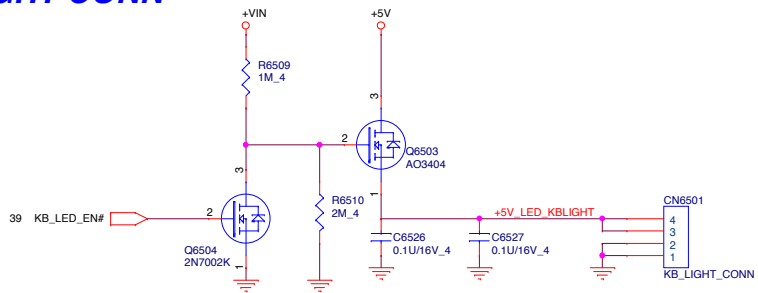
KEYBOARD Con.



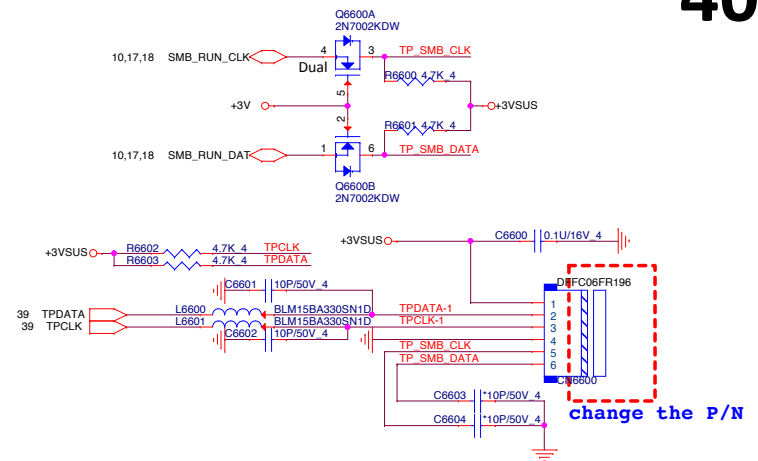
KEYBOARD PULL-UP



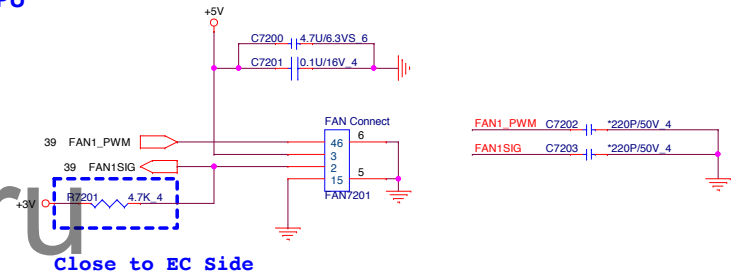
KB LIGHT CONN



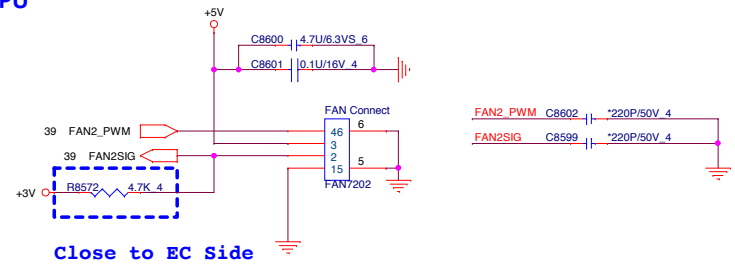
Touch Pad Connector



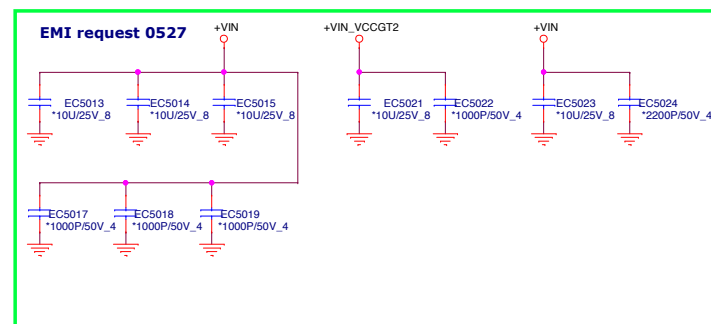
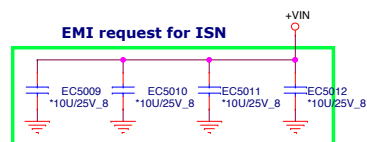
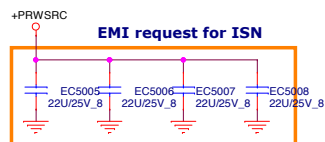
FAN1 for CPU



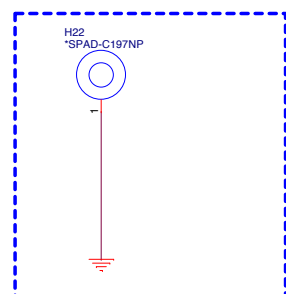
FAN2 for GPU



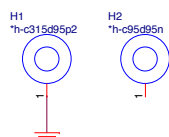




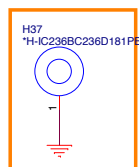
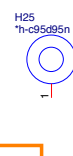
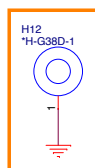
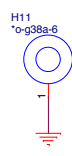
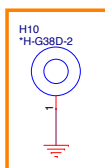
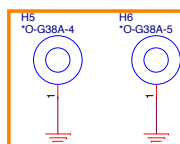
## HOLE



Place to TOP(EMI)

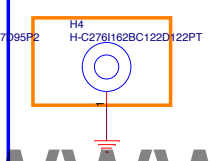


SI change

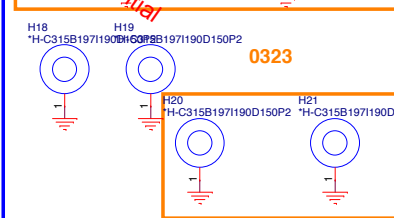
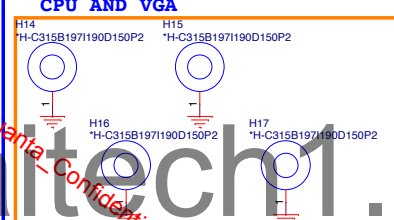


0322

## WLAN NUT on BOT



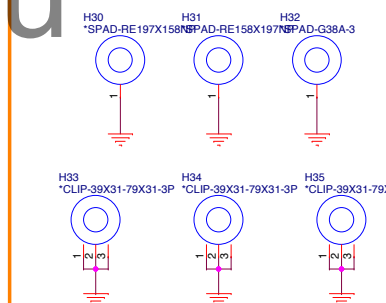
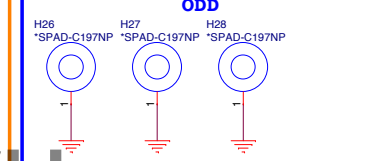
## CPU AND VGA



## PCH NUT on BOT



## ODD



# 1xxx

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DC\_JACK

CN7706

LED2

LED1

LED\_CONN

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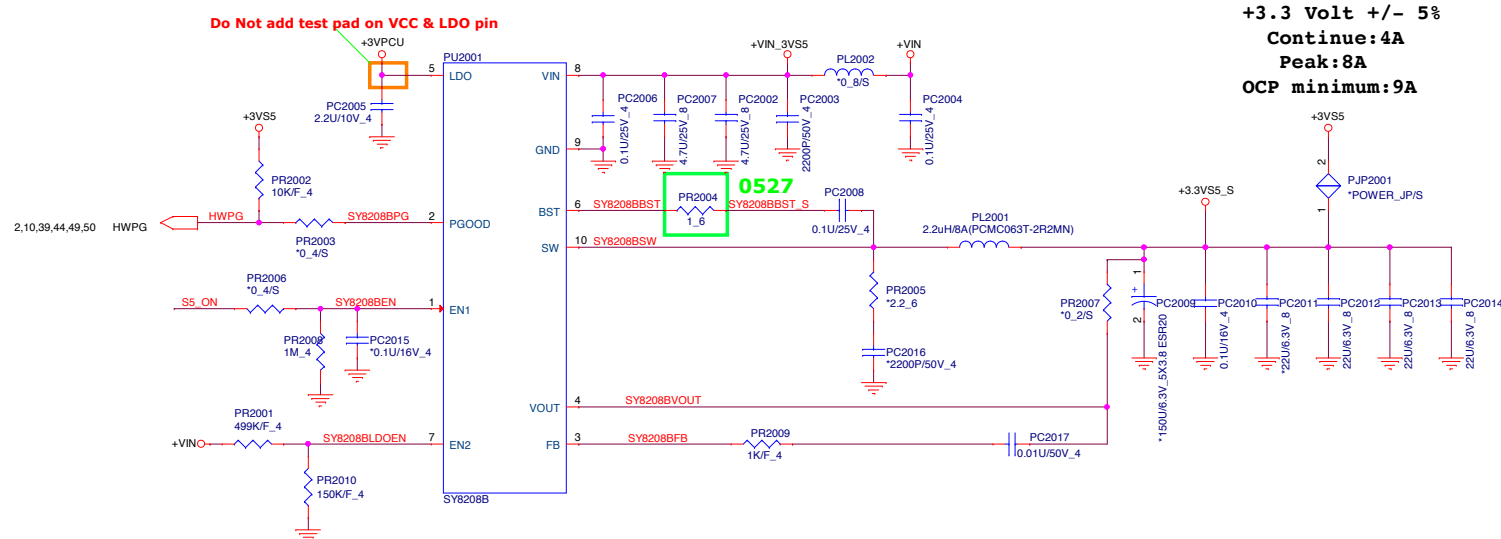
VDD

VDD

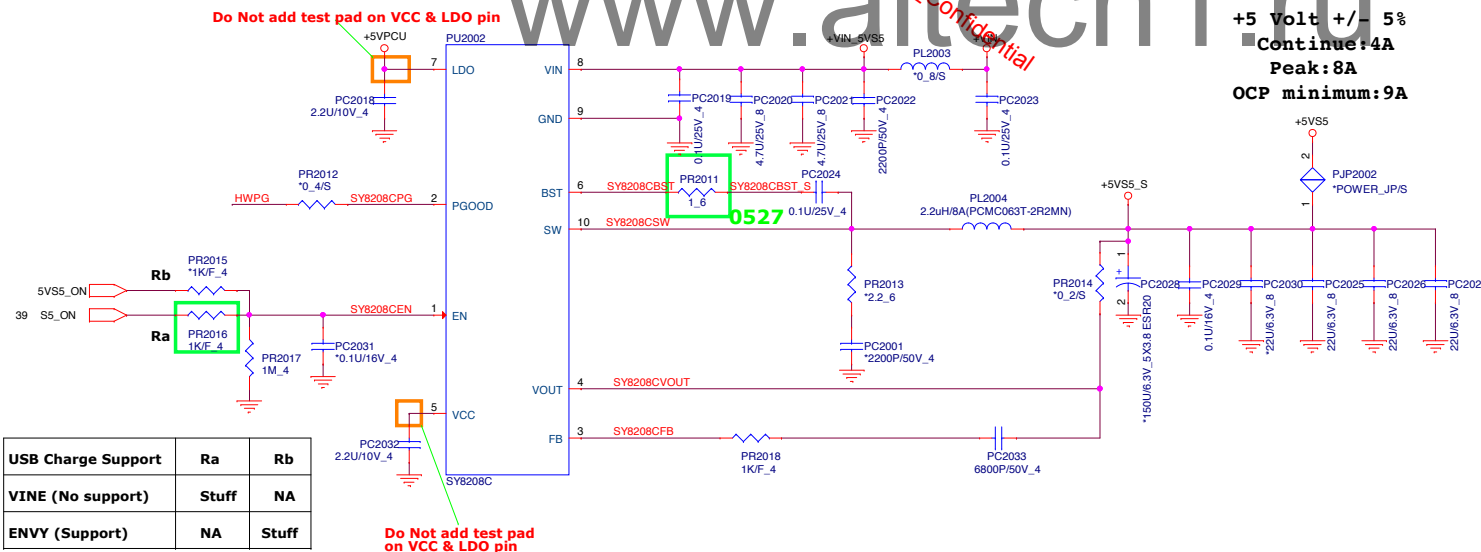
VDD

VDD

2xxx



+3.3 Volt +/- 5%  
Continue:4A  
Peak:8A  
OCP minimum:9A



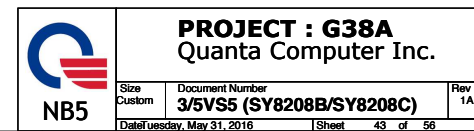
+5 Volt +/- 5%  
 Continue: 4A  
 Peak: 8A  
 OCP minimum: 9A

<b>USB Charge Support</b>	<b>Ra</b>	<b>Rb</b>
<b>VINE (No support)</b>	<b>Stuff</b>	<b>NA</b>
<b>ENVY (Support)</b>	<b>NA</b>	<b>Stuff</b>

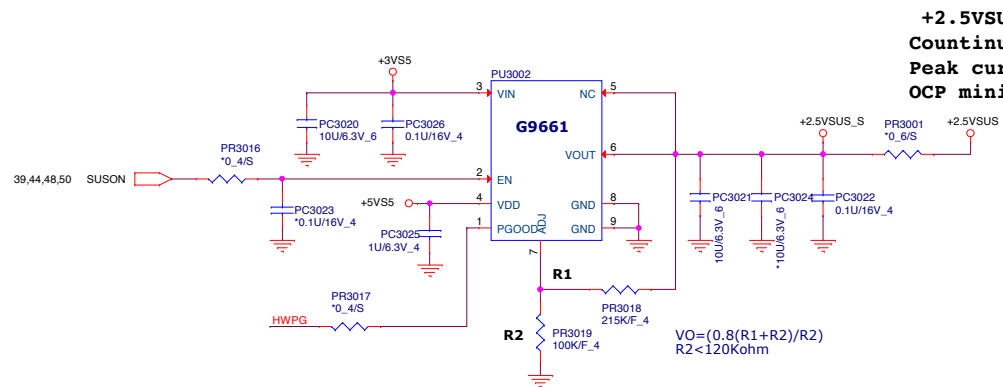
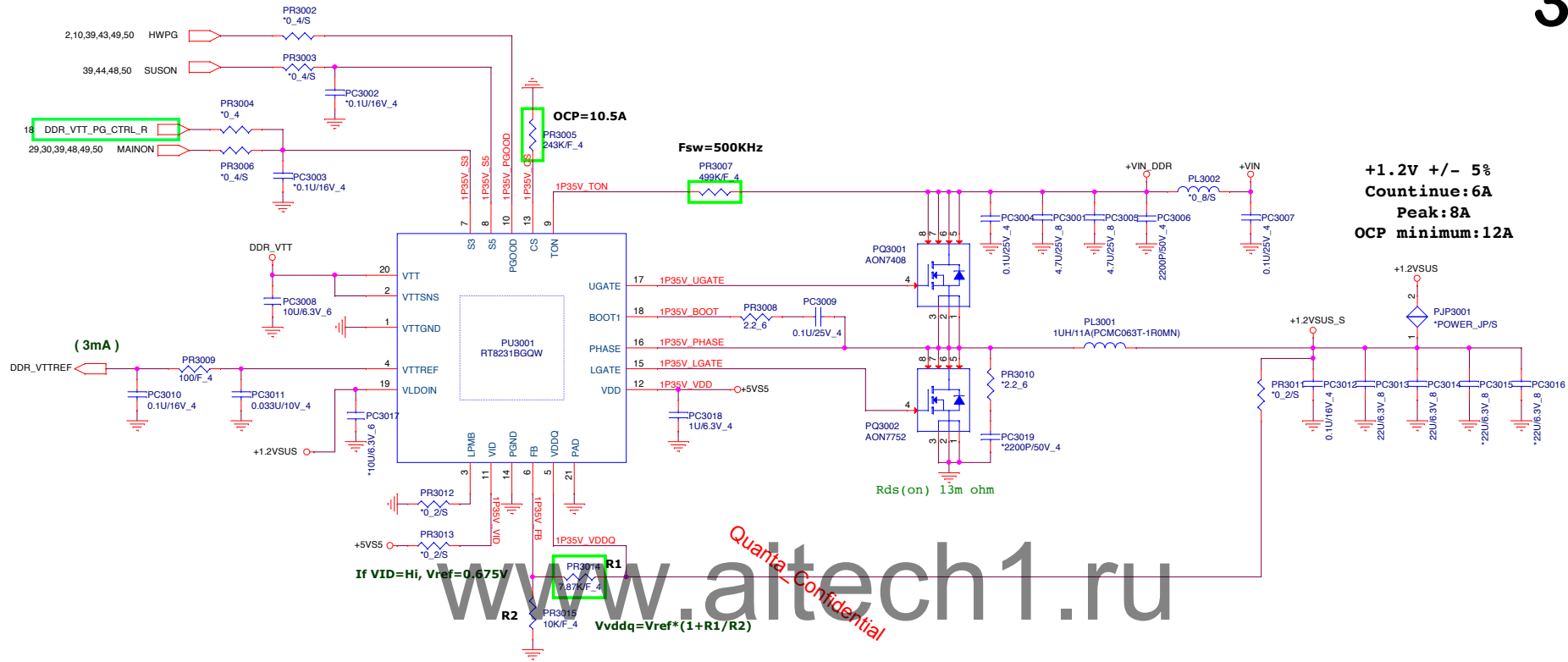
**Do Not add test pad on VCC & LDO pin**

WIN\_5VS5 PL2003 4.8V

+VIN	28,40,41,42,44,45,46,47,48,49,50,51,54
+3VS5	10,12,14,16,28,29,30,35,39,44,48,49,50
+5VS5	10,28,31,33,44,45,46,47,48,49,50,51,52,53,54,55
+3VPCU	5,10,21,33,35,39,40,42,51
+5VPCU	31,42,48,55



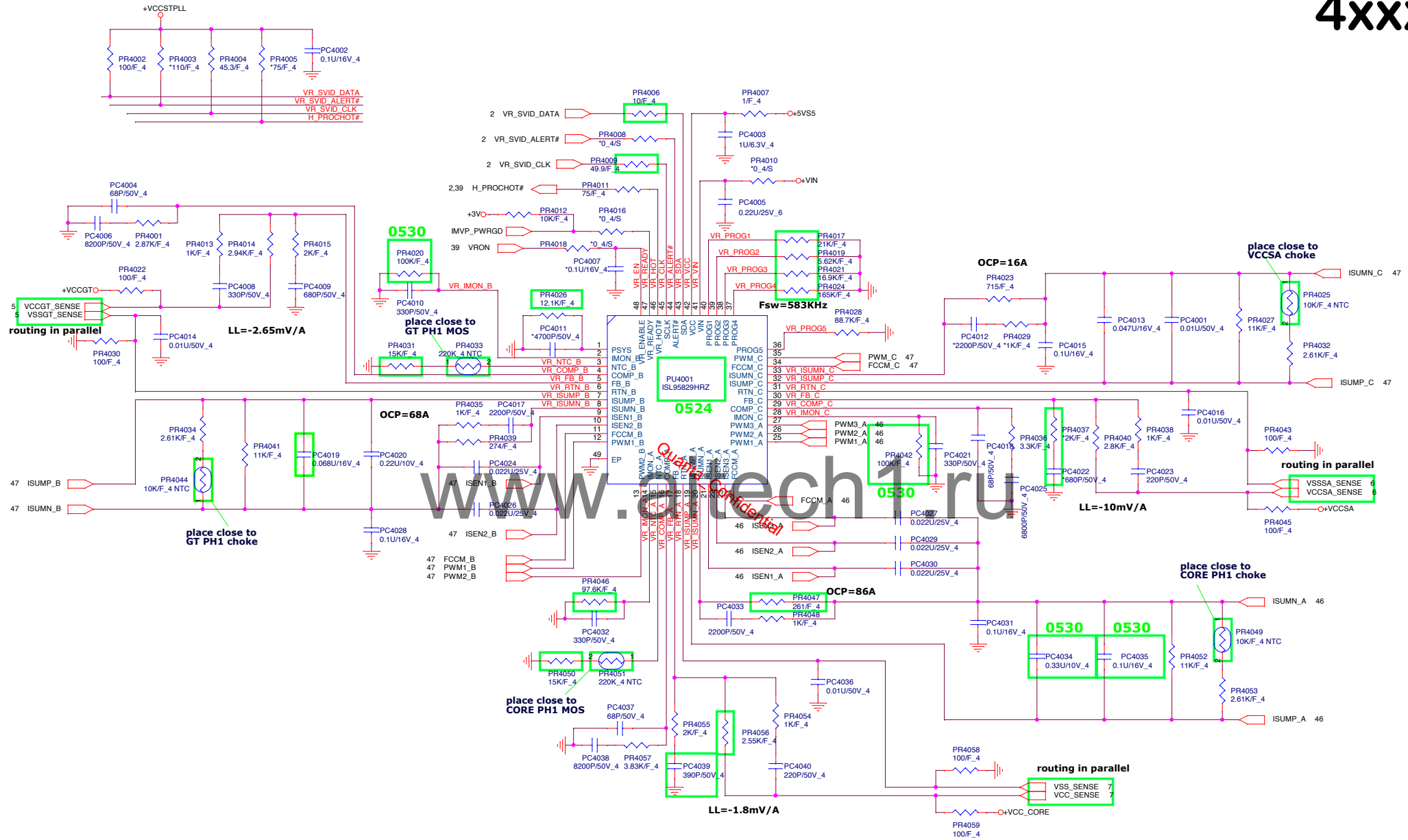
# 3xxx



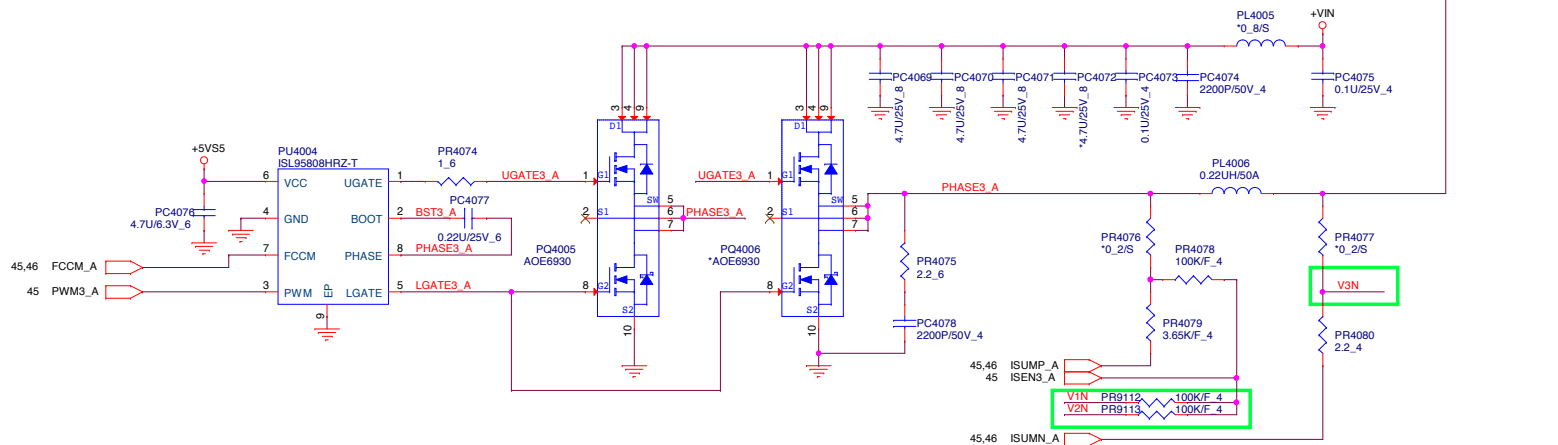
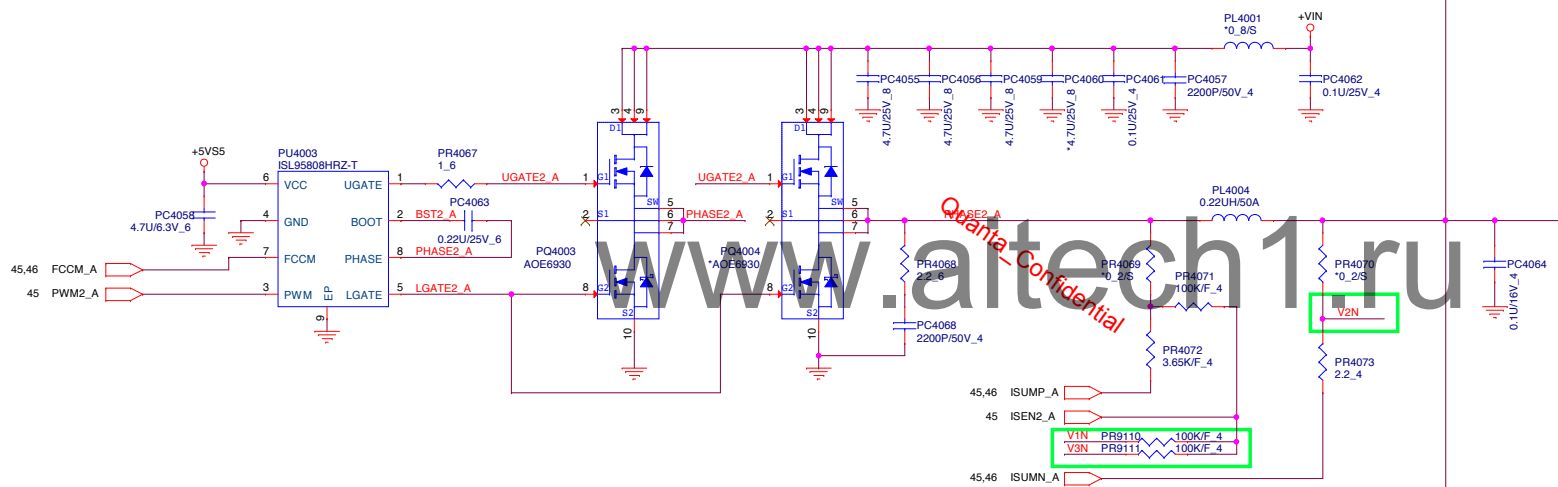
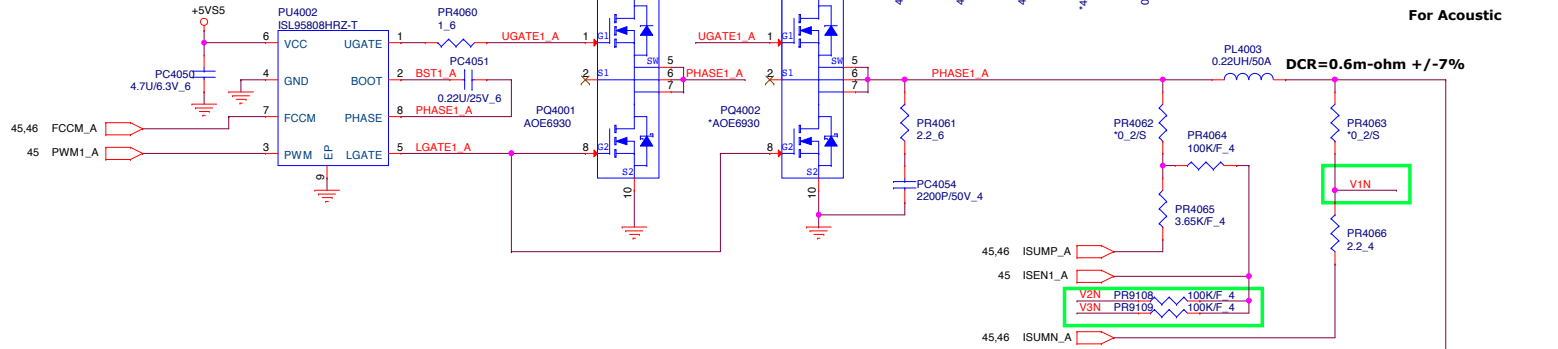
+VIN	28,40,41,42,43,45,46,47,48,49,50,51,54
+5VS5	10,28,31,33,43,45,46,47,48,49,50,51,52,53,54,55
+1.2VSUS	2,6,10,17,18,50,55
DDR_VTT	17,18
+2.5VSUS	17,18

	<b>PROJECT : G38A</b> <b>Quanta Computer Inc.</b>		
	Size	Document Number	Rev
		<b>DDR3 (RT8231B)</b>	<b>1A</b>
Tuesday, 02/01/2016	Sheet 44	of 56	

4xxx



# 4xxx



**H-line42 (35W)**  
**TDC:44A**  
**Iccmax:60A**  
**OCP:86A**  
**Loadline = -1.8 mV/A**

**H-line42 (45W)**  
**TDC:50A**  
**Iccmax:68A**  
**OCP:86A**  
**Loadline = -1.8 mV/A**



H-line42 (35W)

**TDC:25A**

**Iccmax: 55A**

**OCP: 68A**

**Loadline = -2.65 mV/A**

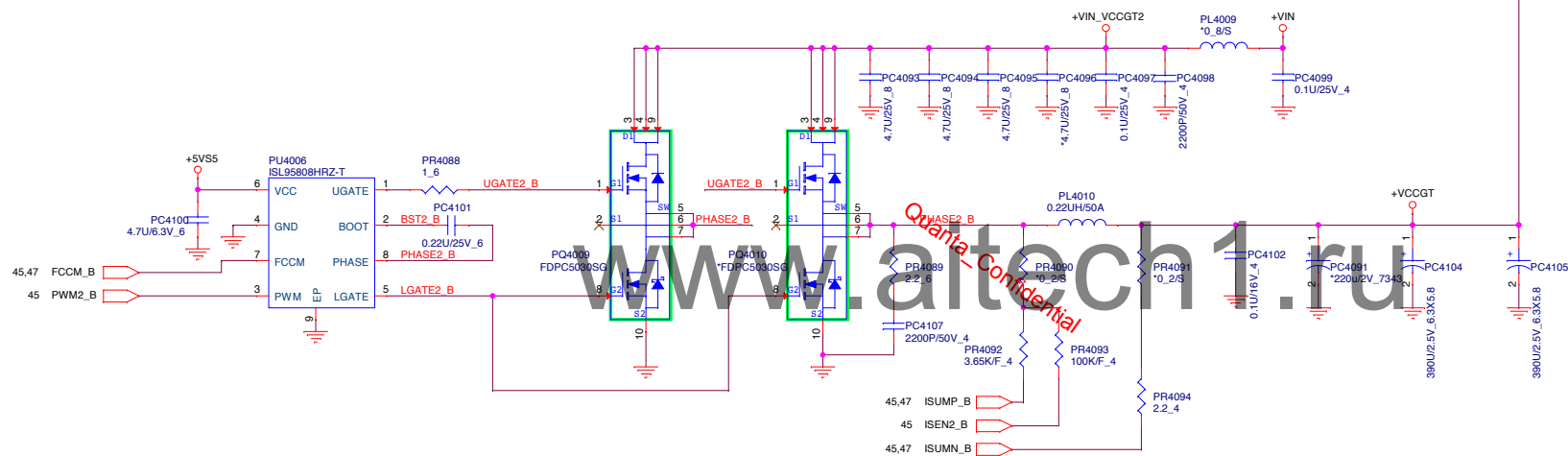
**H-line42 (45W)**

**TDC:25A**

**Iccmax: 55A**

**OCP : 68A**

Loadline = -2.65 mV/A

[illegible]

**PROJECT : G38A**  
**Quanta Computer Inc.**



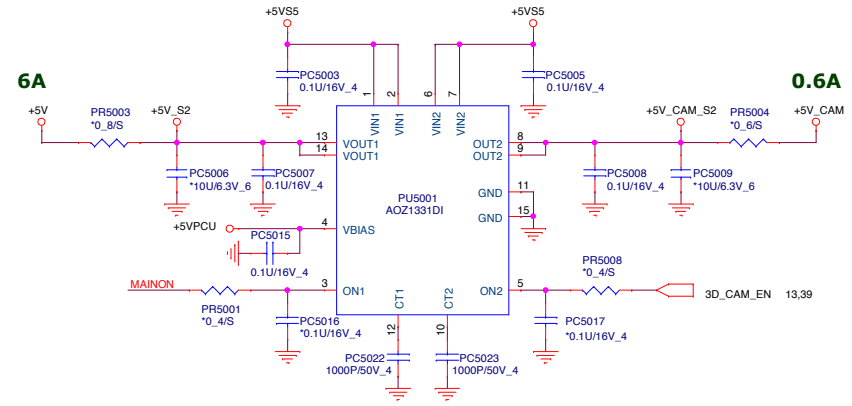
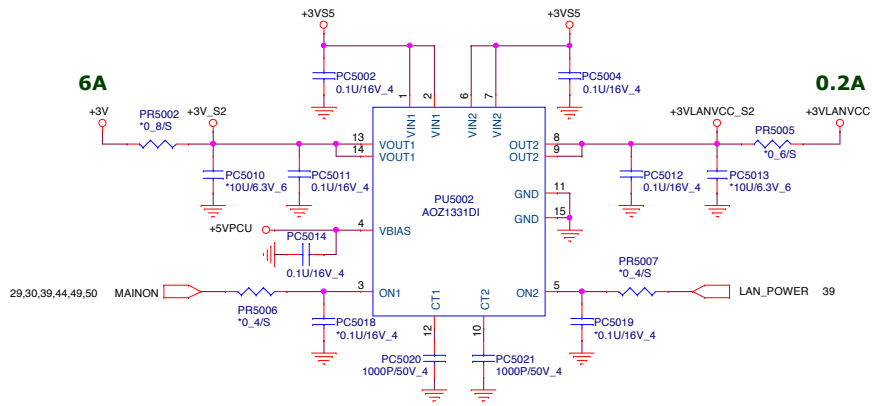
	Size Custom
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Document Number	<b>+VCCGT/SA (ISL95808HRZ-T)</b>
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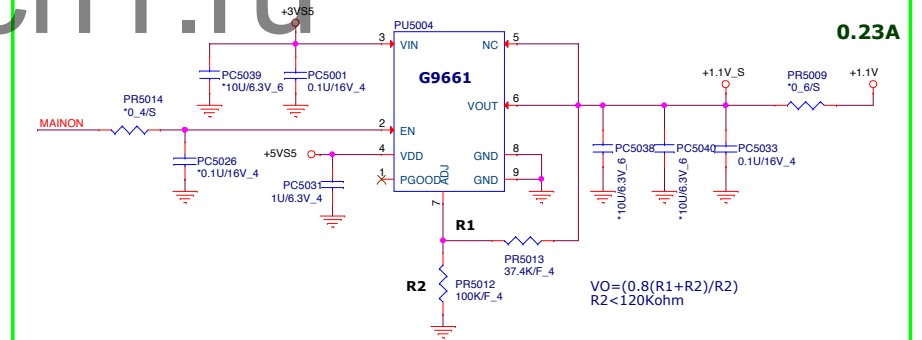
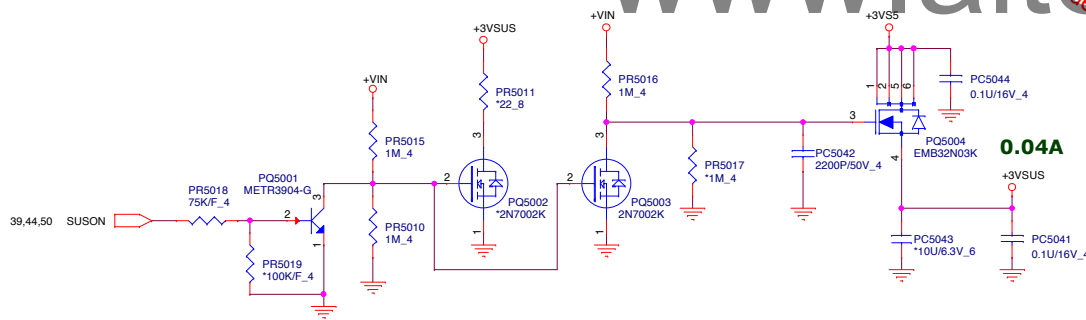
	Rev 1A
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# 5xxx

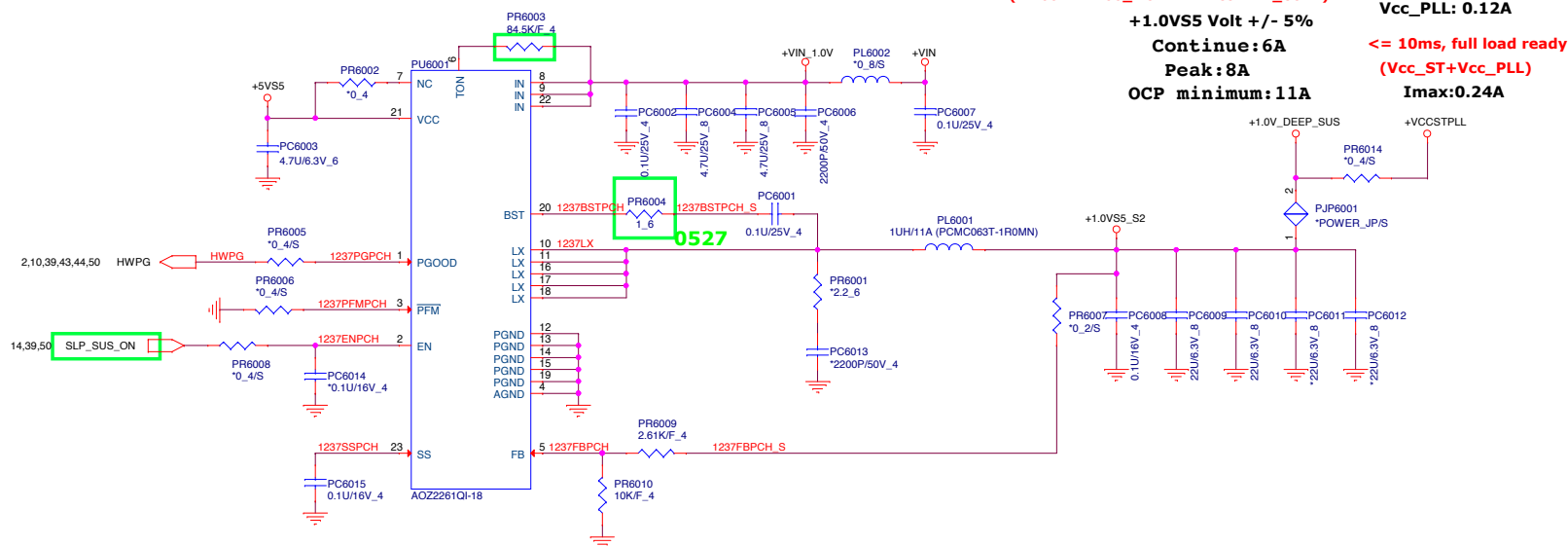


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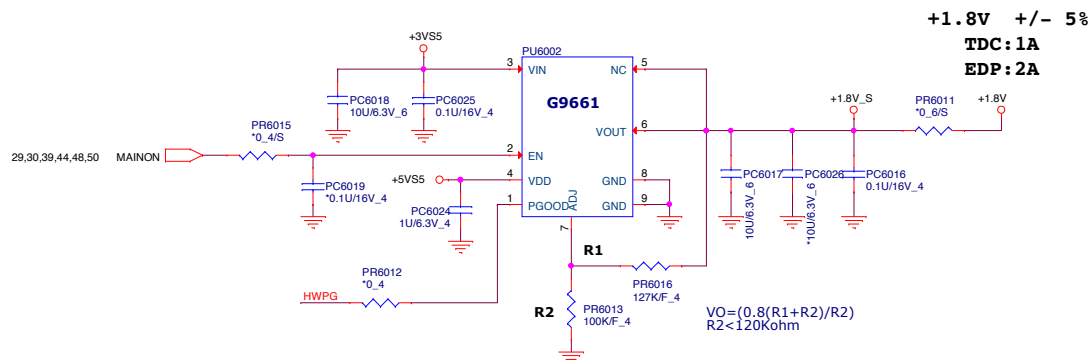


- +3V 5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,54,55
- +5V 28,29,31,32,34,40
- +3VS5 10,12,14,16,28,29,30,35,39,43,44,49,50
- +5VS5 10,28,31,33,43,44,45,46,47,49,50,51,52,53,54,55
- +3VSUS 40
- +3VLAVCC 37
- +5V\_CAM 34

6xxx



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	+VIN	28,40,41,42,43,44,45,46,47,48,50,51,54
	+3VS5	10,12,14,16,28,29,30,35,39,43,44,48,50
	+5VS5	10,28,31,33,43,44,45,46,47,48,50,51,52,53,54,55
	+1.0V_DEEP_SUS	10,11,14,50
	+1.8V	22,31,32,33,34,55
	+VCCSTPLL	2,6,45
	+1.1V	29,48



**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+1.0_DEEP_SUS</b>	Rev 1A
Date:	Tuesday, May 31, 2016	Sheet 49 of 56

# 7xxx

## Volume Segment

Vcc\_STG: 0.04A

Vcc\_IO: 5.5A

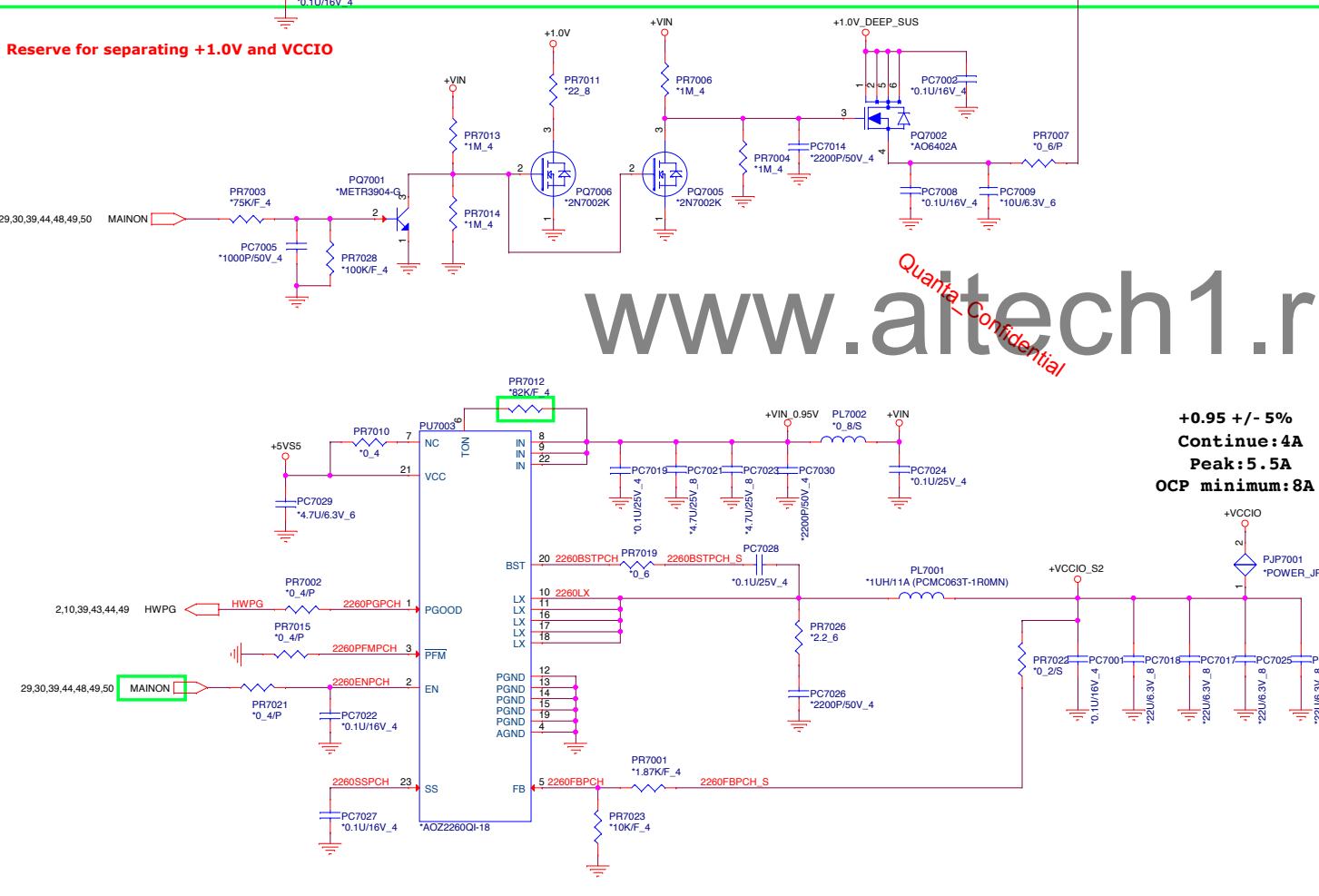
<= 10ms full load ready

Imax:5.5A

Imax:0.04A

<= 240us, full load ready

TDC:0.26A

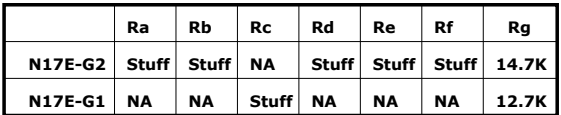


+0.95 +/- 5%  
Continue:4A  
Peak:5.5A  
OCP minimum:8A

+1.0V	2,5,6,10,39
+3VS5	10,12,14,16,28,29,30,35,39,43,44,48,49
+5VS5	10,28,31,33,43,44,45,46,47,48,49,51,52,53,54,55
+VCCIO	3,6
+1.0V_DEEP_SUS	10,11,14,49
+1.2VSUS	2,6,10,17,18,44,55

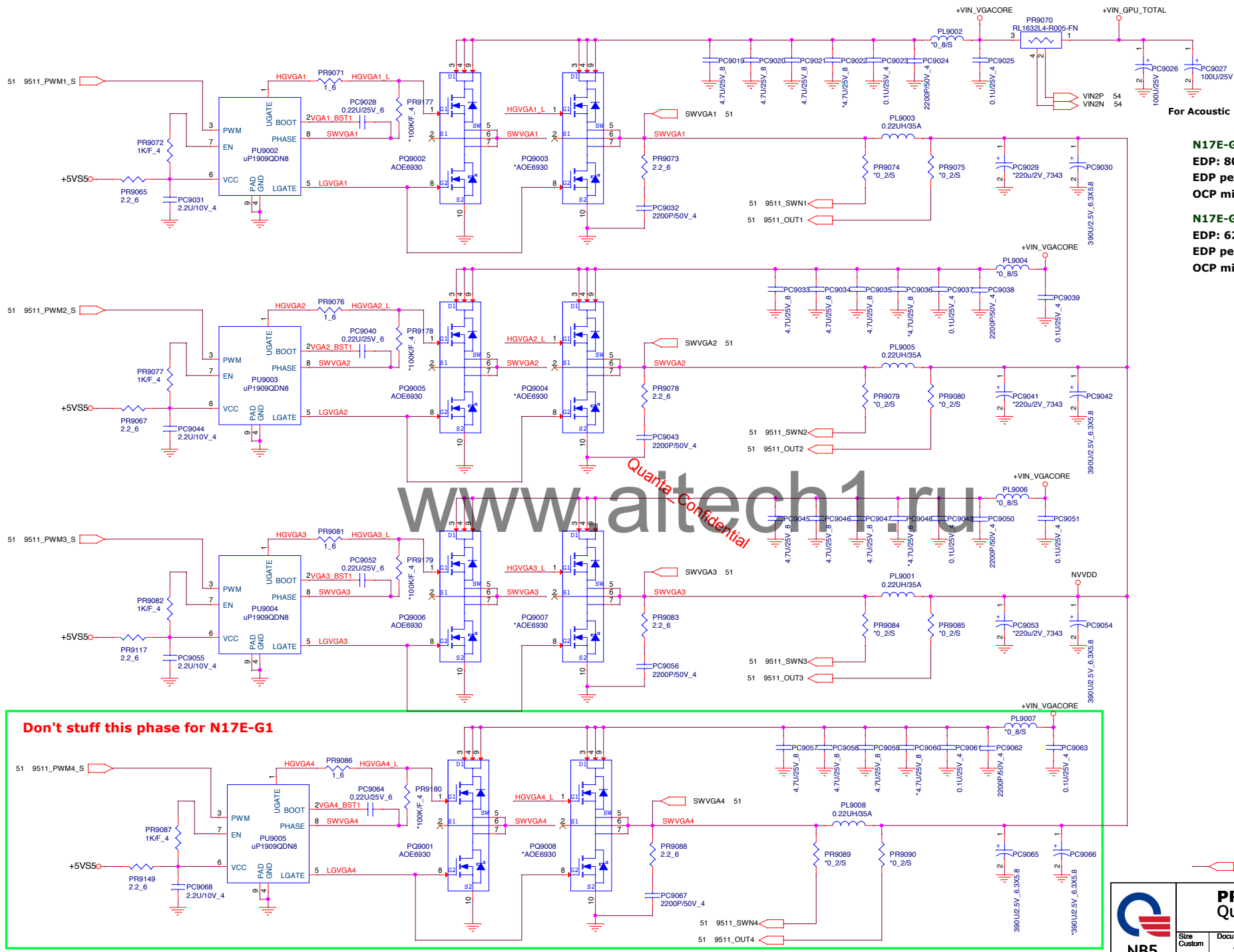
**PROJECT : G38A**  
Quanta Computer Inc.

Size Custom	Document Number <b>+1.0V/+VCCSTPLL/+VCCIO</b>	Rev 1A
Date: Tuesday, May 31, 2016	Sheet 50 of 56	



+3V	5,9,10,11,12,13,14,17,18,21,22,28,29,30,31,32,33,34,35,36,37,38,39,40,45,48,54,55
+VIN	28,40,41,42,43,44,45,46,47,48,49,50,54
+5VS5	10,28,31,33,43,44,45,46,47,48,49,50,52,53,54,55
1V8_AON	19,21,22,53,54,55
NVDD	23,52
1V8_MAIN_EN	21,51,55

# 9xxx



For Acoustic

**N17E-G2 (82W)**  
 EDP: 80A  
 EDP peak: 204A  
 OCP minimum 245A

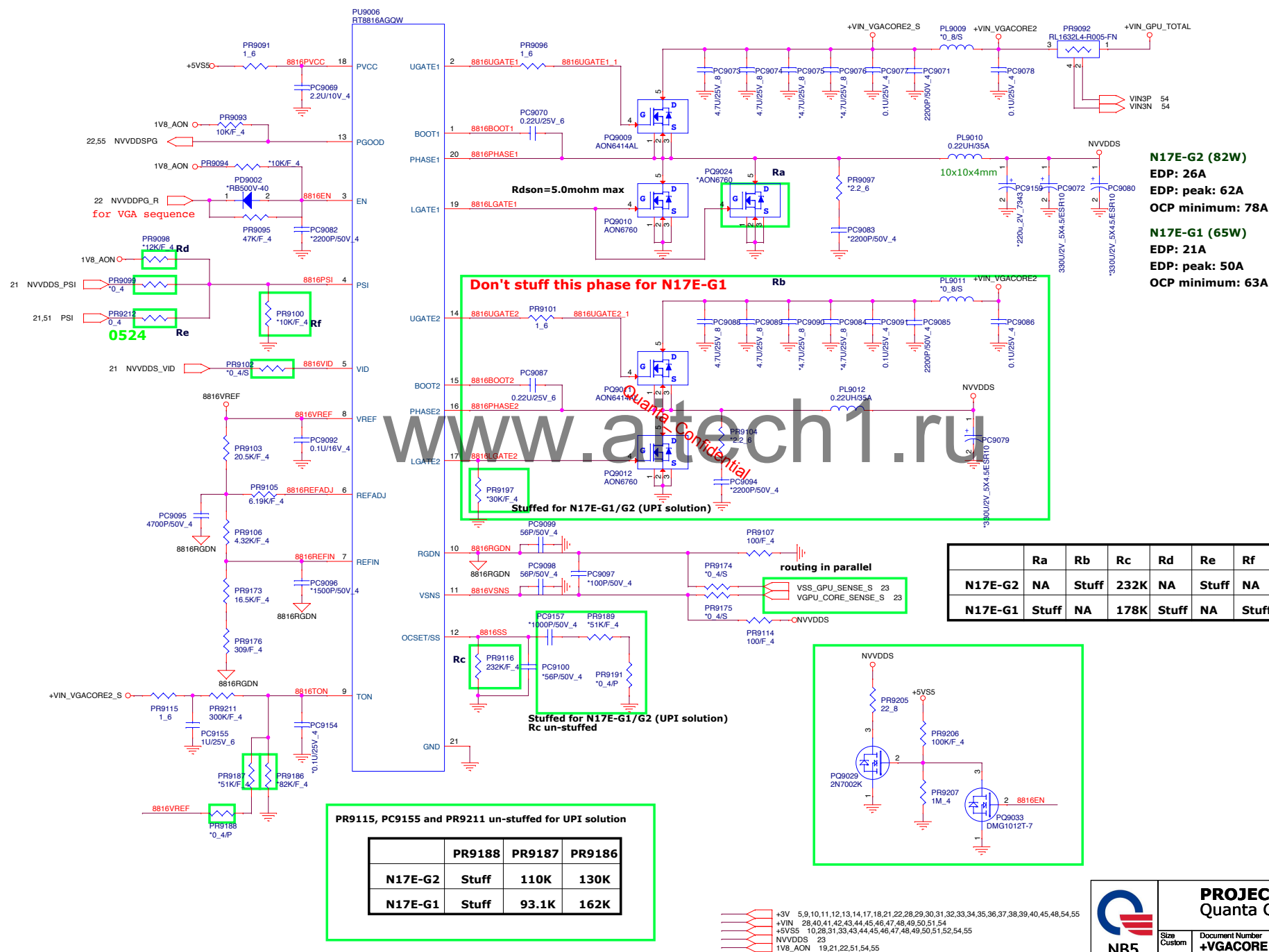
**N17E-G1 (65W)**  
 EDP: 62A  
 EDP peak: 164A  
 OCP minimum 197A

Don't stuff this phase for N17E-G1

**PROJECT : G38A**  
 Quanta Computer Inc.

Size Custom	Document Number <b>+VCORE (NCP81151)</b>	Rev 1A
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# 9xxx

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V/1.5V
0	1.35V

FBVDDQ_MEM	R1	R2
1.55V	35.7K	53.6K
1.5V	30.9K	69.8K

PR9142, PC9156 and PR9145 un-stuffed for UPI solution

	PR9196	PR9195	PR9194
N17E-G2	Stuff	93.1K	162K
N17E-G1	Stuff	93.1K	162K

Stuffed for N17E-G1/G2 (UPI solution)

Stuffed for N17E-G1/G2 (UPI solution)  
PR9147 un-stuffed

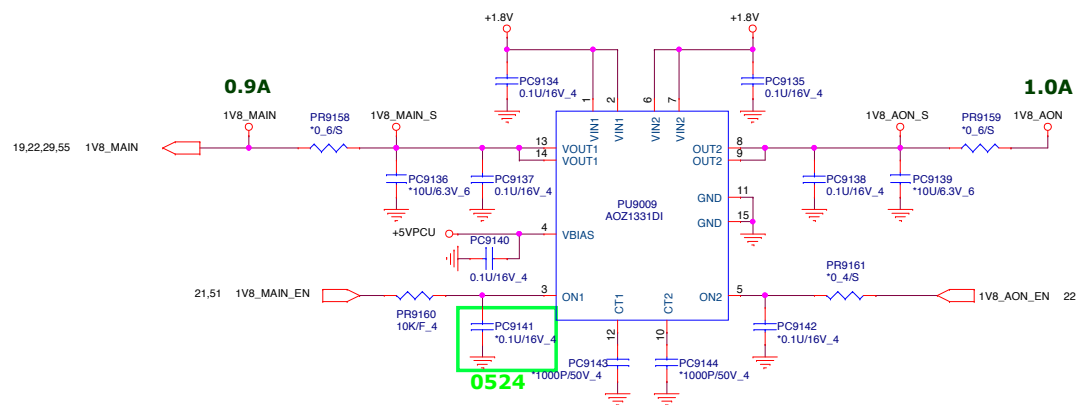
**1.35V/1.55V +/- 5%**  
**N17E-G2 (82W)**  
**EDP: 29A**  
**EDP peak: 53A**  
**OC minimum: 64A**  
**N17E-G1 (65W)**  
**EDP: 25.2A**  
**EDP peak: 46A**  
**OC minimum: 64A**



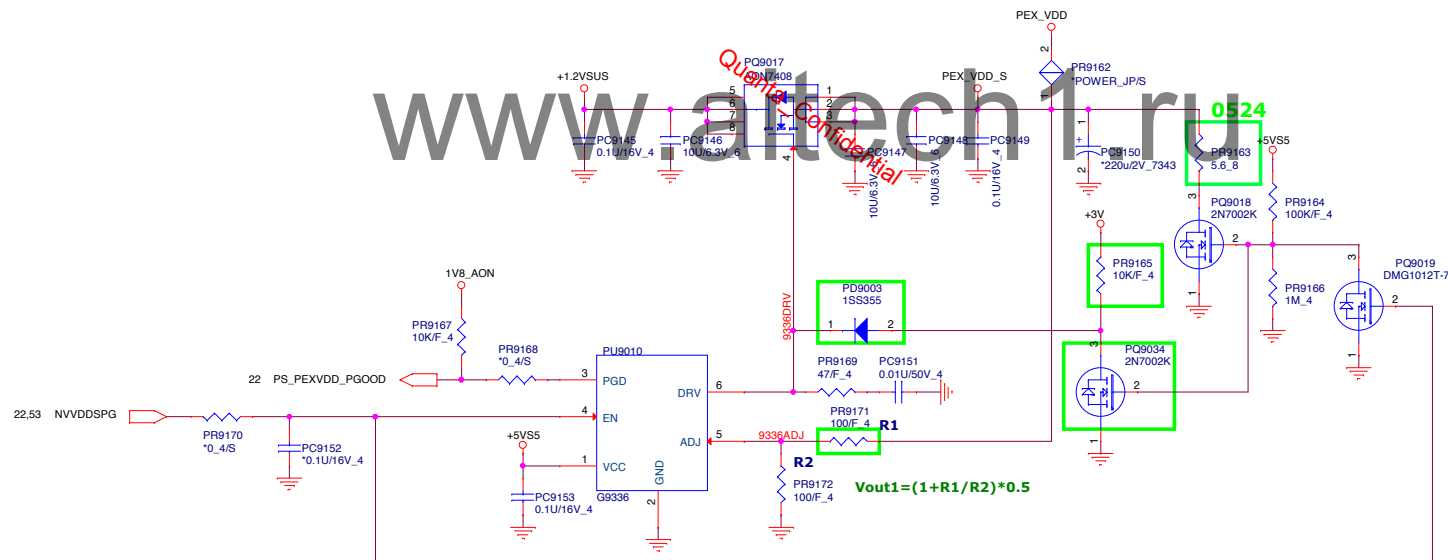
**PROJECT : G38A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>+1.35V_GFX (A0Z2263QI-18)</b>	1A
Date: Tuesday, May 31, 2016	Sheet 54 of 56	

# 9xxx

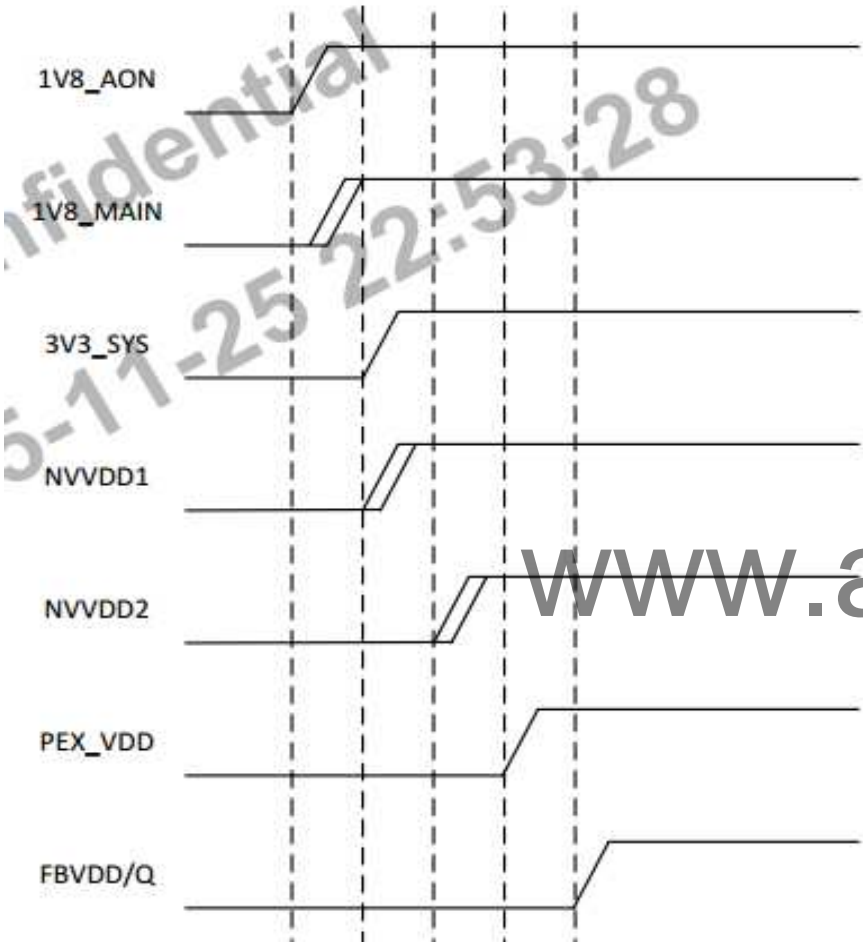


**+1.0V +/- 5%**  
**EDP=2.67A**  
**EDP\_peak = 2.93A**



+VIN 28,40,41,42,43,44,45,46,47,48,49,50,51,54  
 +3VSS 10,12,14,16,28,29,30,35,39,43,44,48,49,50  
 +5VSS 10,28,31,33,43,44,45,46,47,48,49,50,51,52,53,54  
 1V8\_MAIN 19,22,29,55  
 1V8\_AON 19,21,22,51,53,54  
 +1.2VSUS 2,6,10,17,18,44,50  
 PEX\_VDD 19,21

N17E-G2 Power on sequence



N17E-G2 Power off sequence

NVVDDS--->PEX--->NVVDD/FBVDDQ  
----->1V8\_MAIN----->1V8\_AON